

Project Name : A14RMXX REV:1.0

Platform : AMD Danube (Champlain RS880M SB820M)

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25. EXT_MIC/H_P/USB_CHG/G-SEN/3G
26. HDD/ODD /MINI CARD
27. LAN/CARD JMC251 / 30PIN CONN
28. TP/LED/WebCam/FAN
29. EC IT8500BX/BIOS/KB CONN
30. VCC SW
31. DC IN/BT/HOLE/HIGH-SPEED CAP
32. BATT IN/CHARGER(OZ8602)
33. CPU CORE/CPU_VDDNB(OZ8380)
34. +1.1VS(OZ8116)/+0.75VS/+1.8V
35. +1.5VS/+5VA (OZ815)/+3.3VA
36. +CPU_VDDR/+2.5V
37. Reserved

CPU

NB

SB

M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note
2010.04.09	A	71R-A14RM0-4BA0	BTI	64R-A14RM1-00A0	
		71R-A14RM0-9HA0	HANDSTAR		
		71R-A14RM0-T8A0	TTL		
2010.05.19	A1	71R-A14RM0-4BA1	BTI	64R-A14RM1-00A1	
		71R-A14RM0-T8A1	TTL		
2010.05.20	B			64R-A14RM1-00B0	
				64R-A14RM1-10B0	
				64R-A14RM1-20B0	

Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

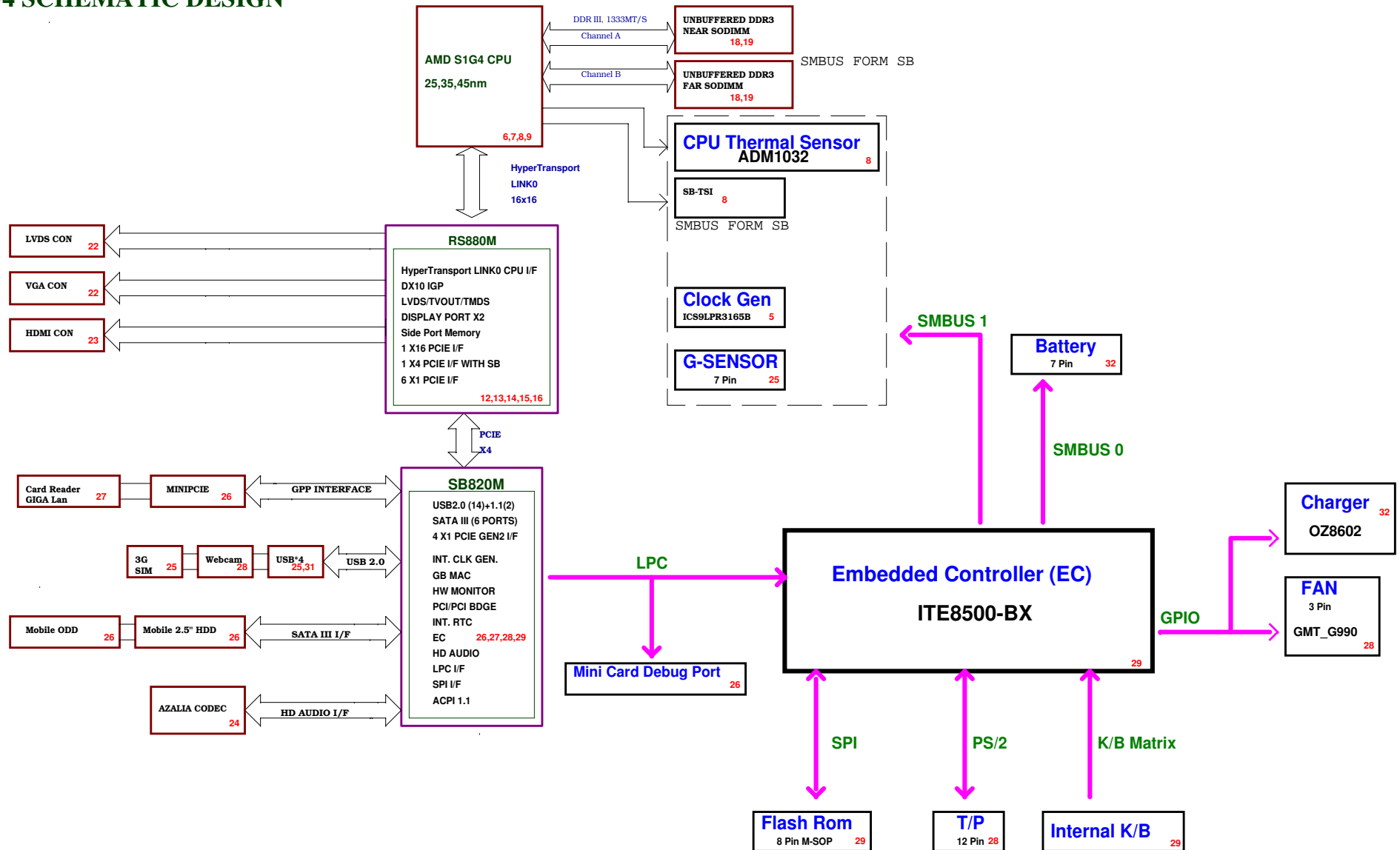
Shuttle Inc

A14RM

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Custom		
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SYSTEM BLOCK DIAGRAM

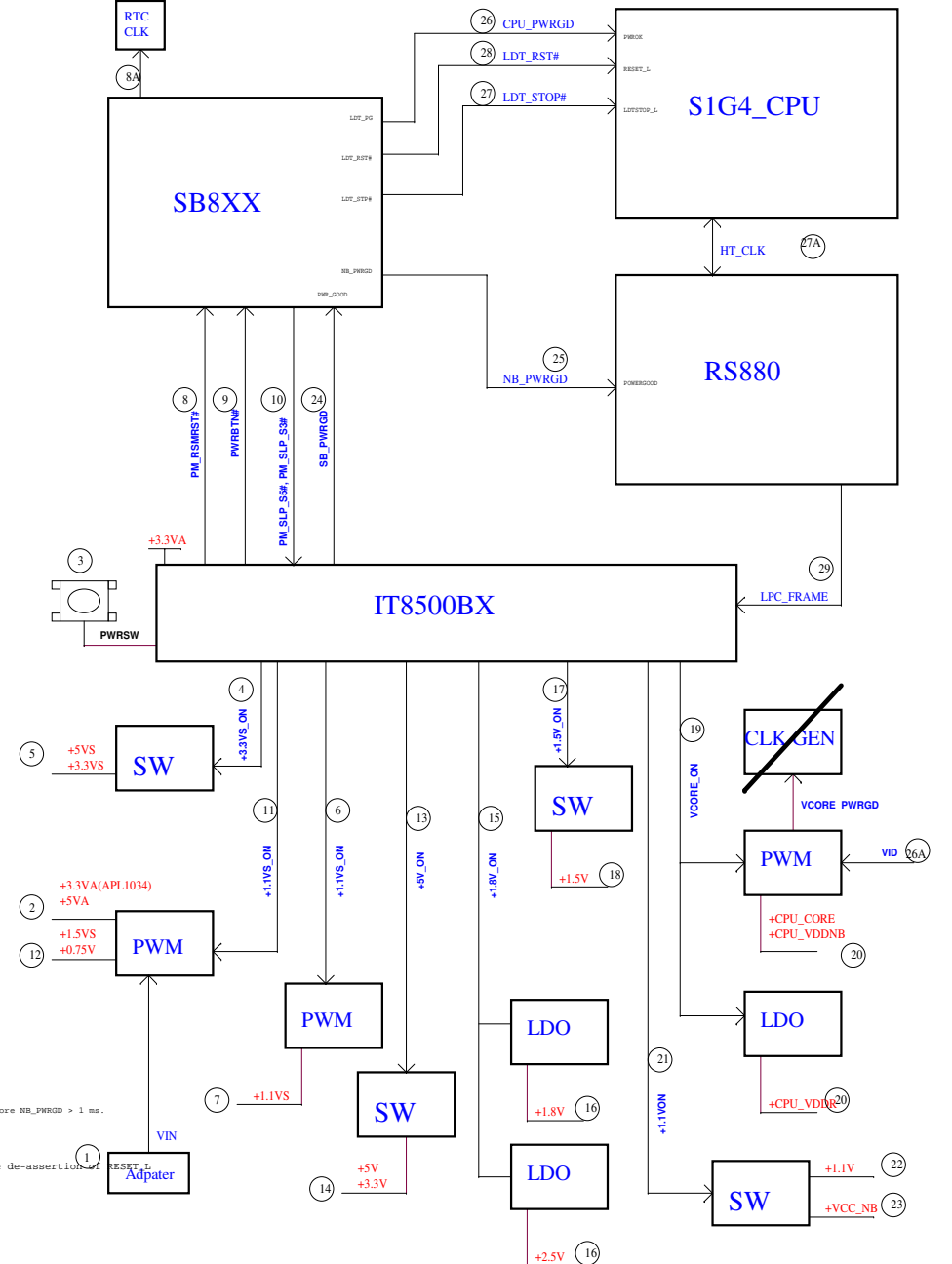
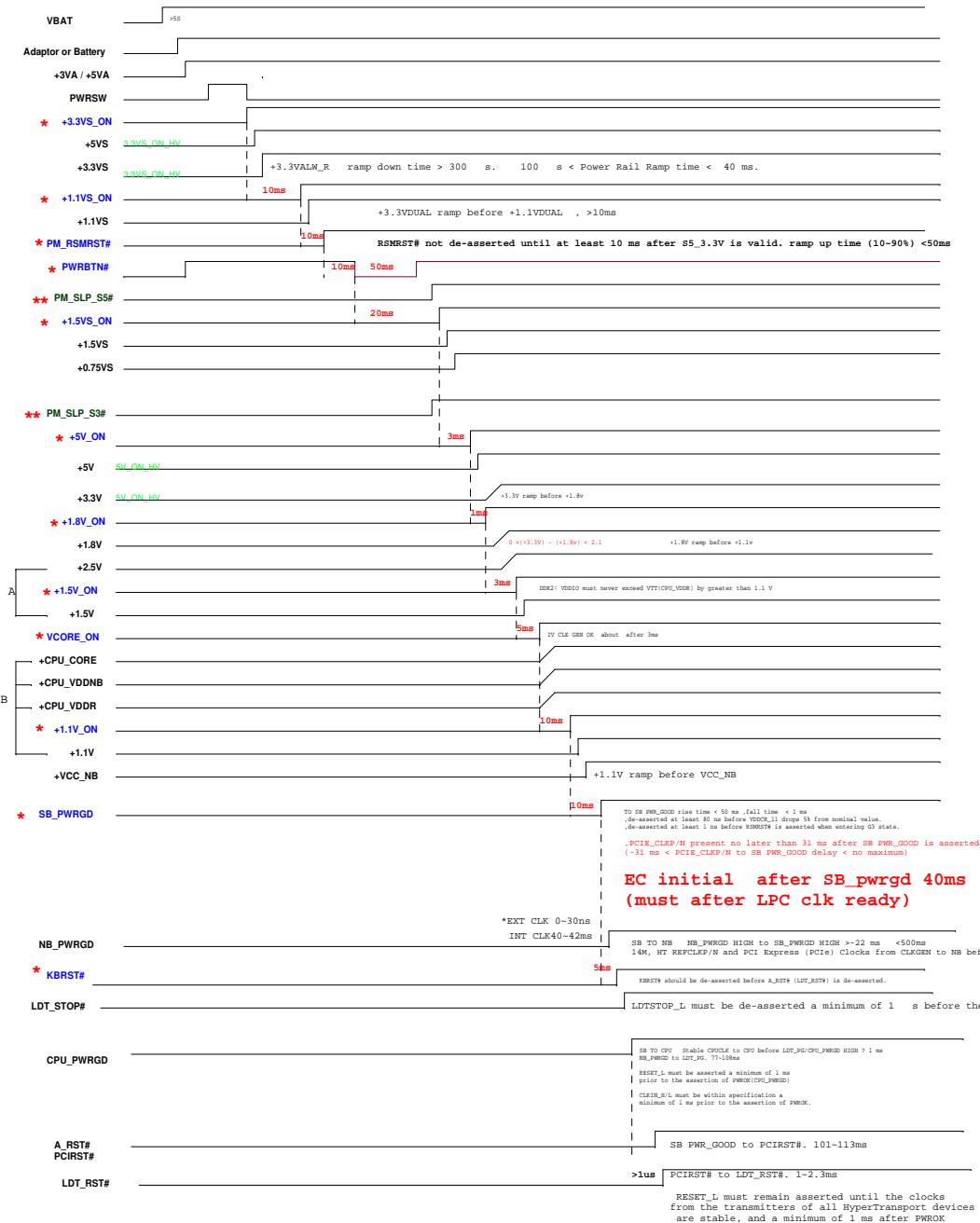
S1G4 SCHEMATIC DESIGN



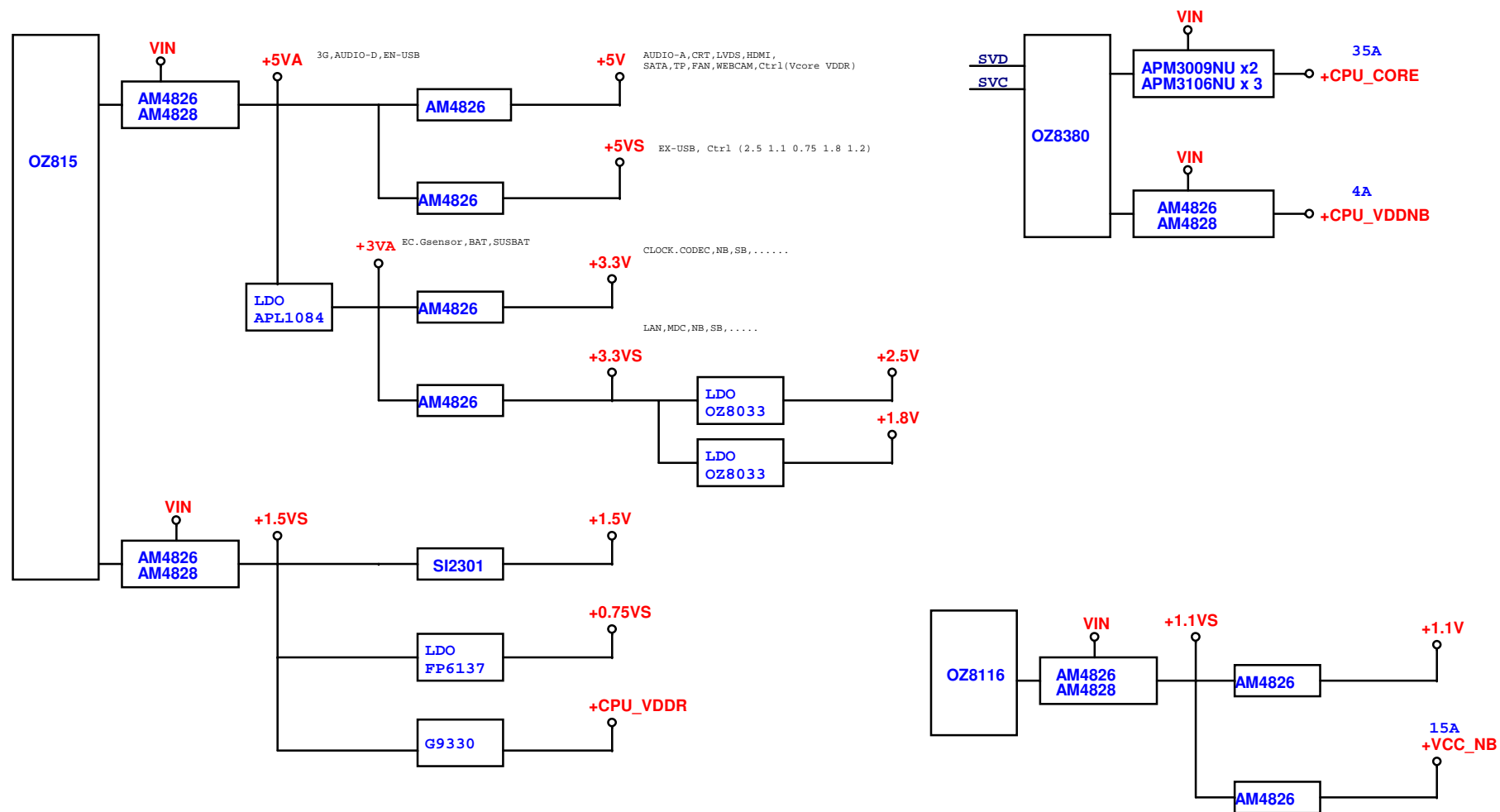
System Power On Sequence

- * EC Control Pin (O/P)
- ** EC Control Pin(I/P)

ALL POWER --> 50 s < Power Rail Ramp time < 40 ms.

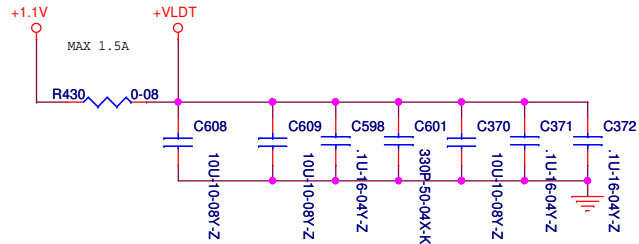
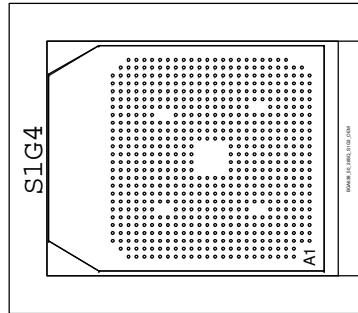


POWER BLOCK DIAGRAM



MB_13

use internal clk gen



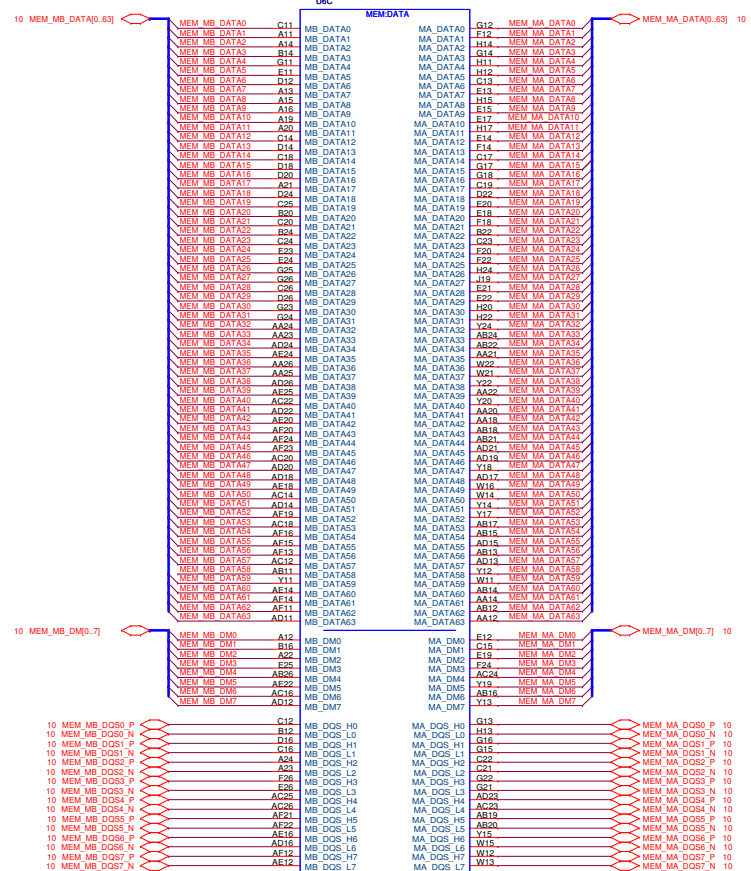
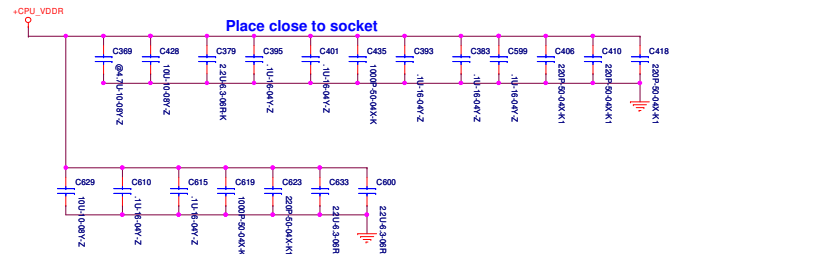
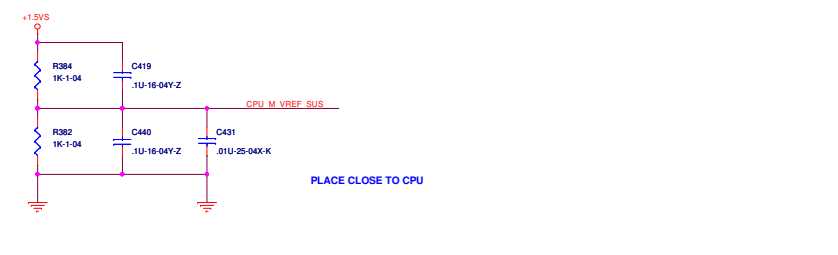
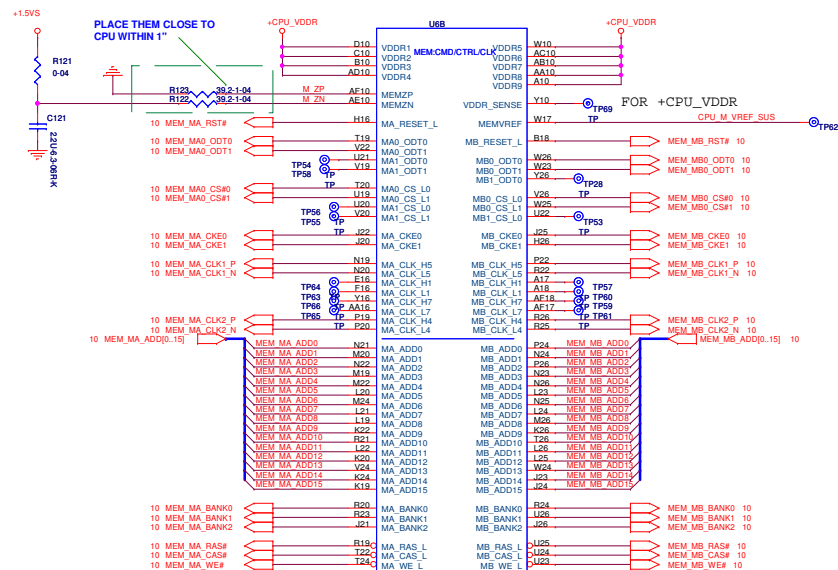
Place close to socket

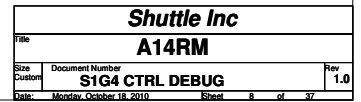
12 HT_NB_CPU_CAD_H0
12 HT_NB_CPU_CAD_L0
12 HT_NB_CPU_CAD_H1
12 HT_NB_CPU_CAD_L1
12 HT_NB_CPU_CAD_H2
12 HT_NB_CPU_CAD_L2
12 HT_NB_CPU_CAD_H3
12 HT_NB_CPU_CAD_L3
12 HT_NB_CPU_CAD_H4
12 HT_NB_CPU_CAD_L4
12 HT_NB_CPU_CAD_H5
12 HT_NB_CPU_CAD_L5
12 HT_NB_CPU_CAD_H6
12 HT_NB_CPU_CAD_L6
12 HT_NB_CPU_CAD_H7
12 HT_NB_CPU_CAD_L7
12 HT_NB_CPU_CAD_H8
12 HT_NB_CPU_CAD_L8
12 HT_NB_CPU_CAD_H9
12 HT_NB_CPU_CAD_L9
12 HT_NB_CPU_CAD_H10
12 HT_NB_CPU_CAD_L10
12 HT_NB_CPU_CAD_H11
12 HT_NB_CPU_CAD_L11
12 HT_NB_CPU_CAD_H12
12 HT_NB_CPU_CAD_L12
12 HT_NB_CPU_CAD_H13
12 HT_NB_CPU_CAD_L13
12 HT_NB_CPU_CAD_H14
12 HT_NB_CPU_CAD_L14
12 HT_NB_CPU_CAD_H15
12 HT_NB_CPU_CAD_L15
12 HT_NB_CPU_CLK_H0
12 HT_NB_CPU_CLK_L0
12 HT_NB_CPU_CLK_H1
12 HT_NB_CPU_CLK_L1
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12 HT_NB_CPU_CTL_L0
12 HT_NB_CPU_CTL_H1
12 HT_NB_CPU_CTL_L1

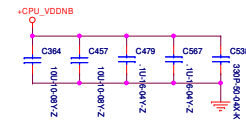
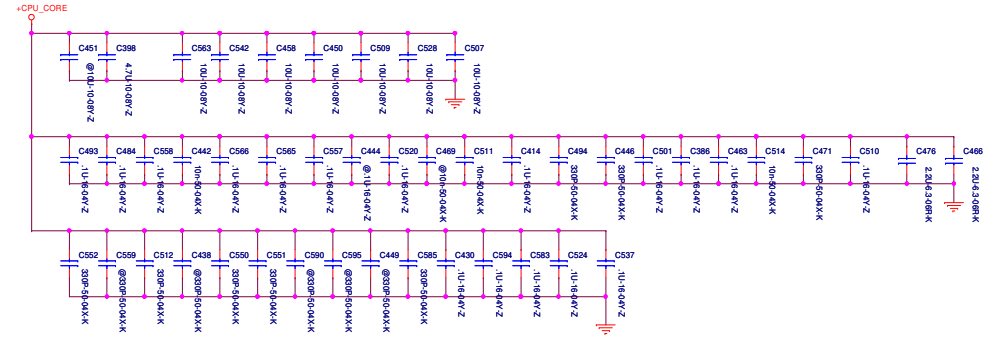


con_cpu638_pz6382a-284s-41f_fox

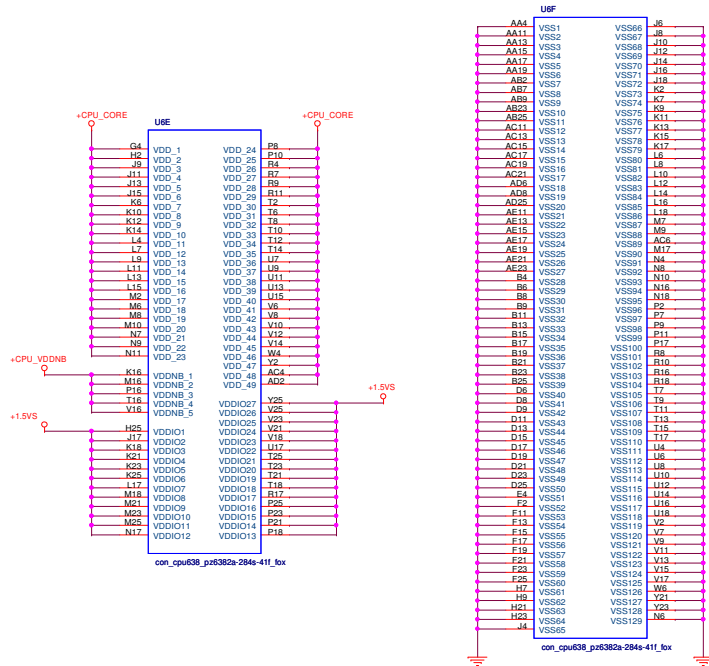
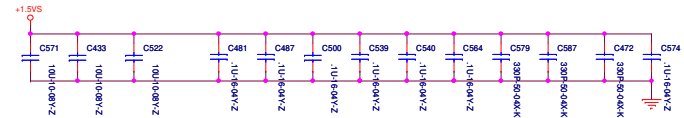
Processor Memory Interface



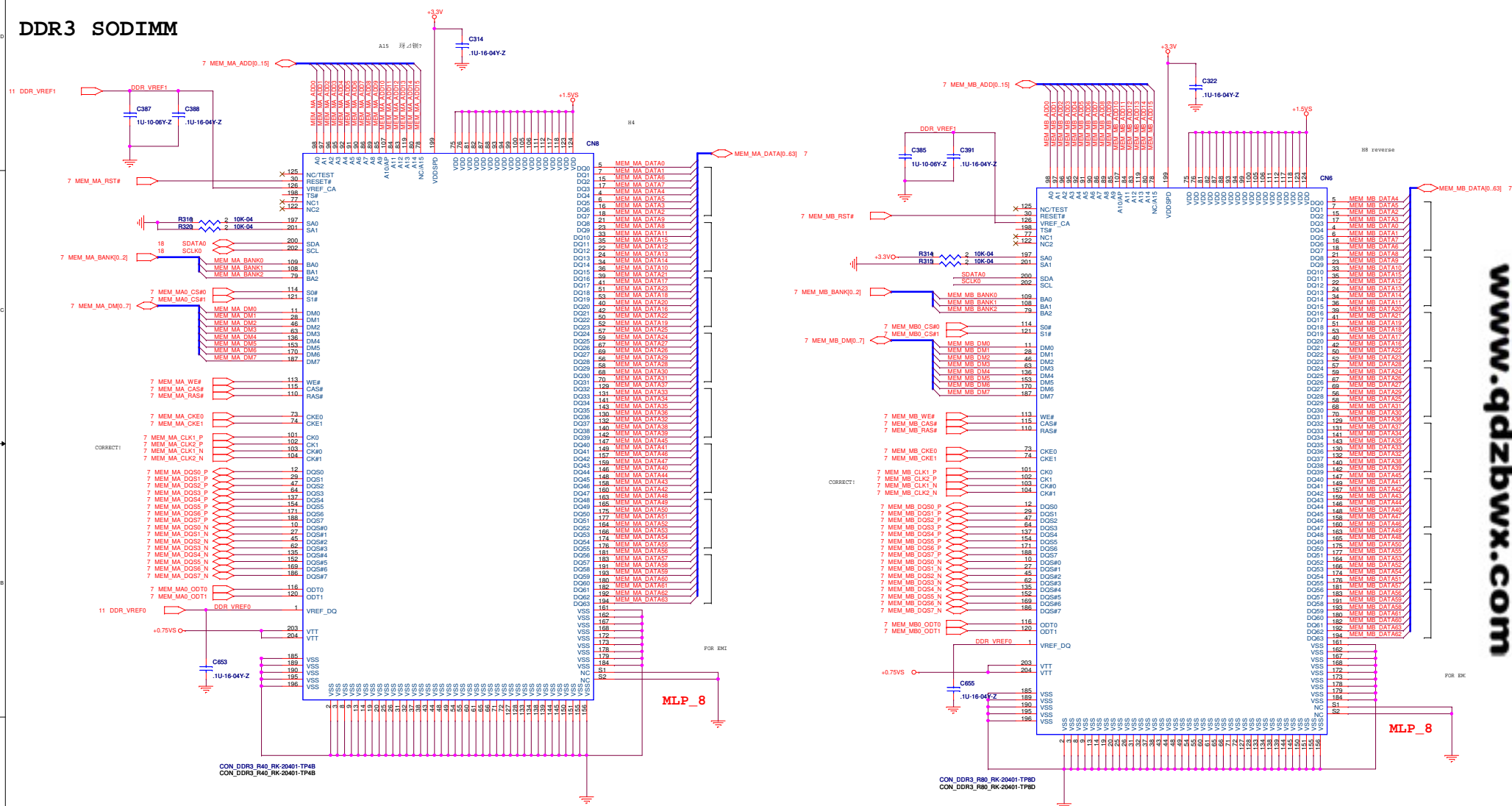




DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE



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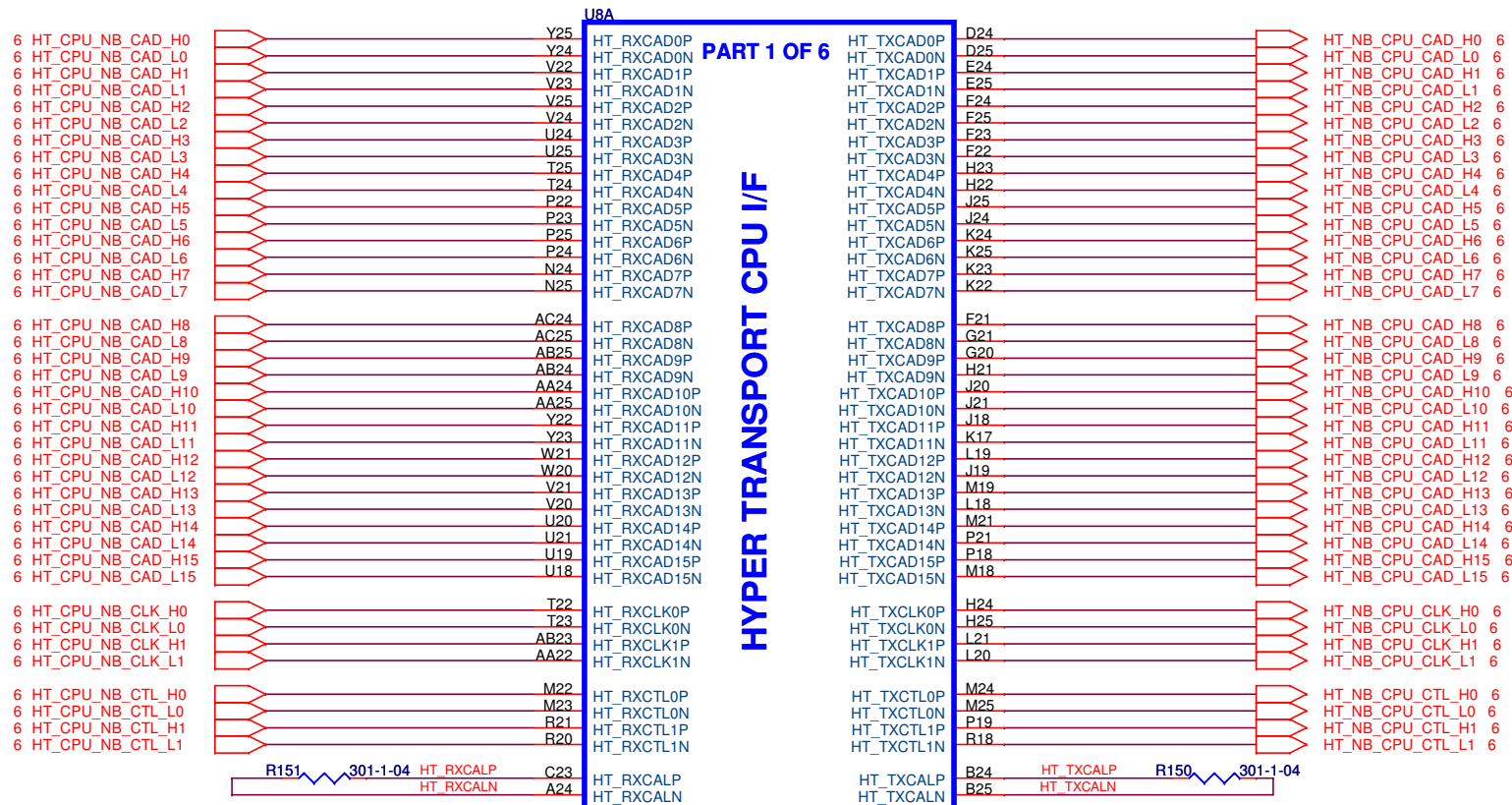
D

D

C

B

A



U8A

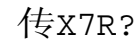
PART 1 OF 6

HYPER TRANSPORT CPU I/F

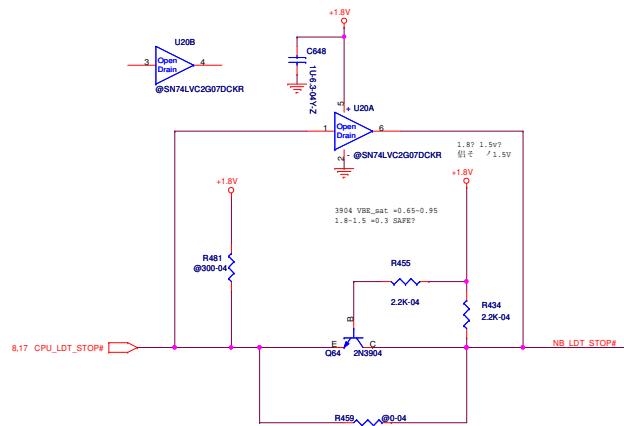
216-0752001

VLP_2

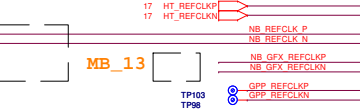
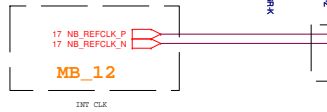
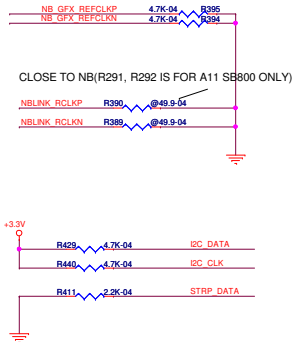
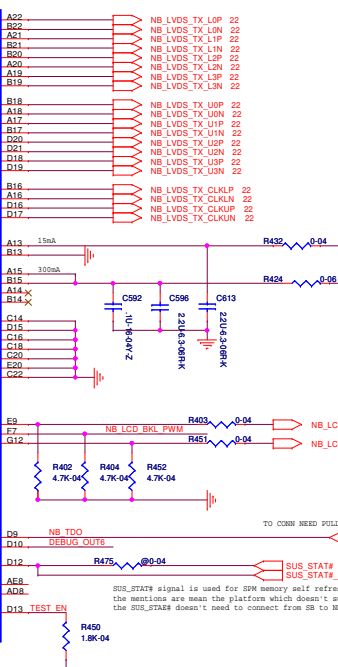
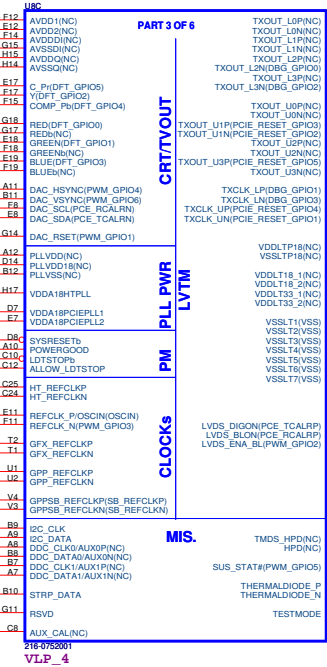
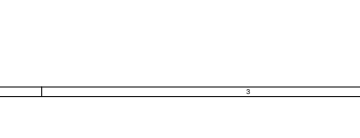
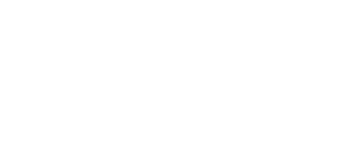
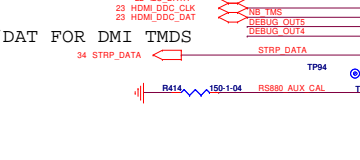
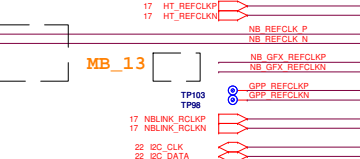
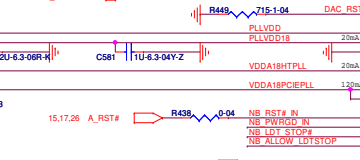
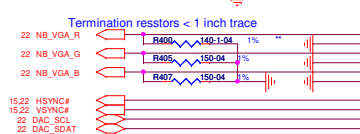
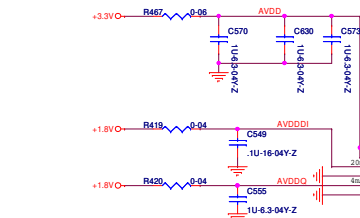
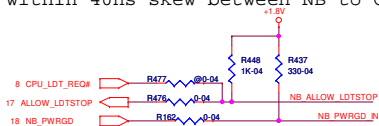
MXM3.0 need put the CAP on the motherboard.
Close to the MXM Slot



All PCIe lane should route 8" max for Gen2 connector and max 12" for Gen2 on board devices
Guam has the Lasso lane over 8" due to the large board, should use shorter lasso cable for Guam....
Customer need to follow the MBDG.



require within 40ns skew between NB to CPU



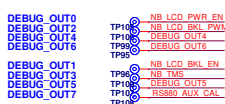
DDC_CLK/DAT FOR DMI TMD5

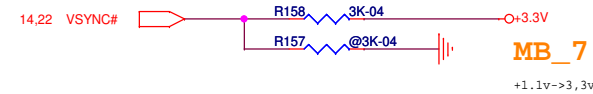
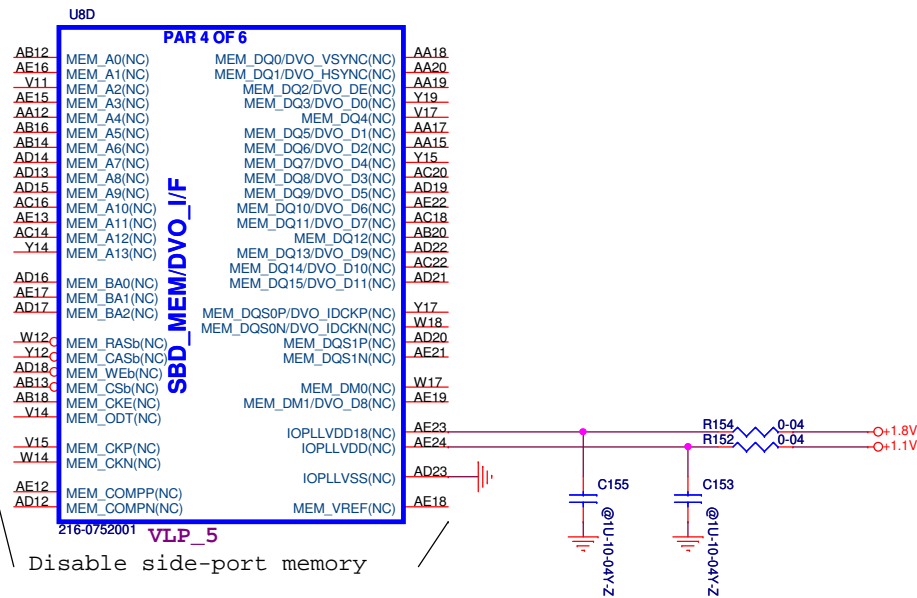
34 STRP_DATA

RS880M JTAG

RS880M DEBUG PIN MAPPING

DEBUG_OUT0	LVDS_DIGON
DEBUG_OUT1	LVDS_ENA_BL
DEBUG_OUT2	LVDS_BLON
DEBUG_OUT3	TMD5_HPD
DEBUG_OUT4	AUXIN
DEBUG_OUT5	AUX1P
DEBUG_OUT6	HPD
DEBUG_OUT7	AUX_CAL





STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

RS880M	
1 Disable	
0 Enable	



Disable side-port memory

??

RS880M: Enables Side port memory

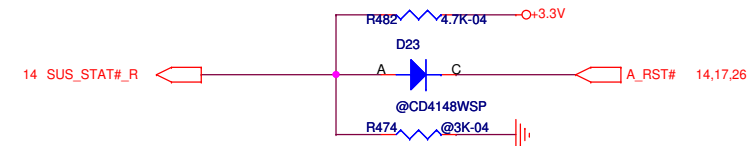
RS880M:HSYNC#

Selects if Memory SIDE PORT is available or not

1 = Memory Side port Not available

0 = Memory Side port available

Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values

0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

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Title

Size Custom

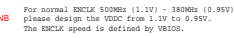
Document Number

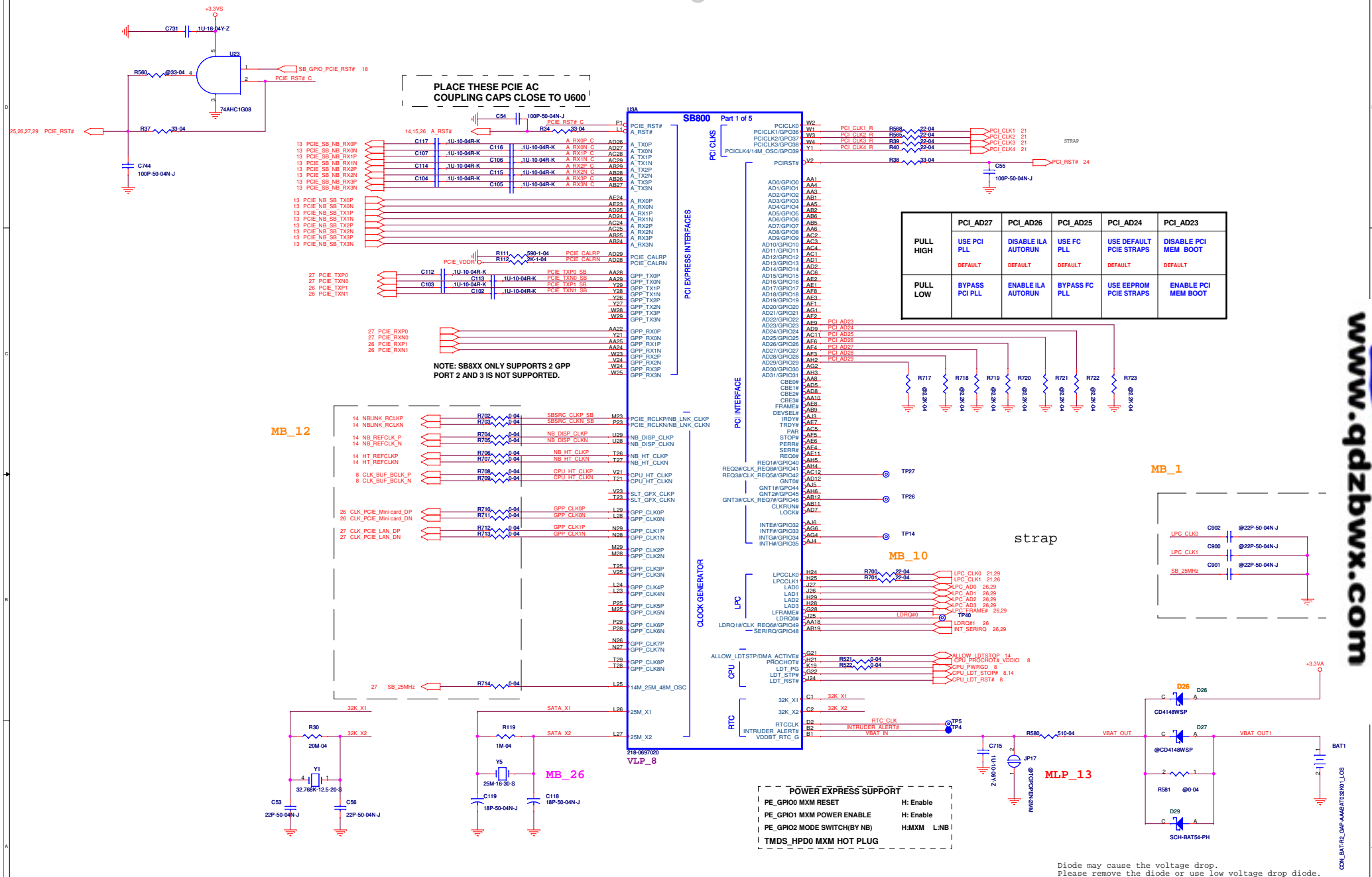
RS880M SPMEM STRAP

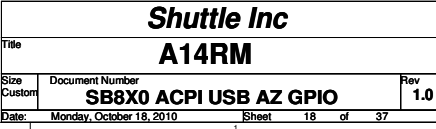
Rev 1.0

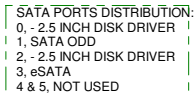
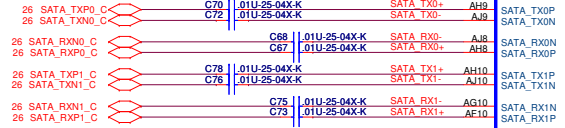
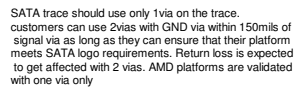
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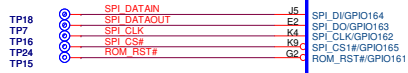
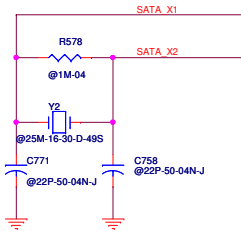
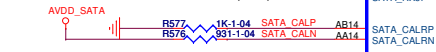






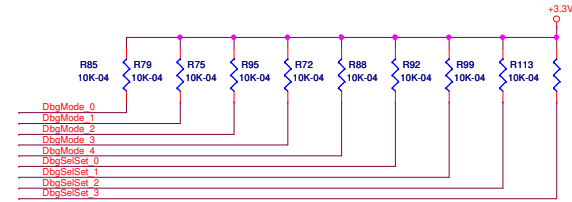
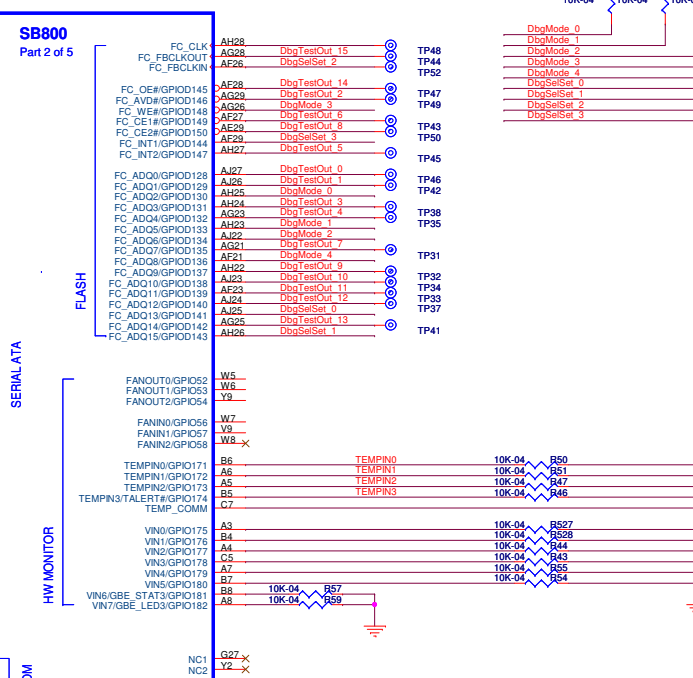
PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF U600

REV: A12 (1K)



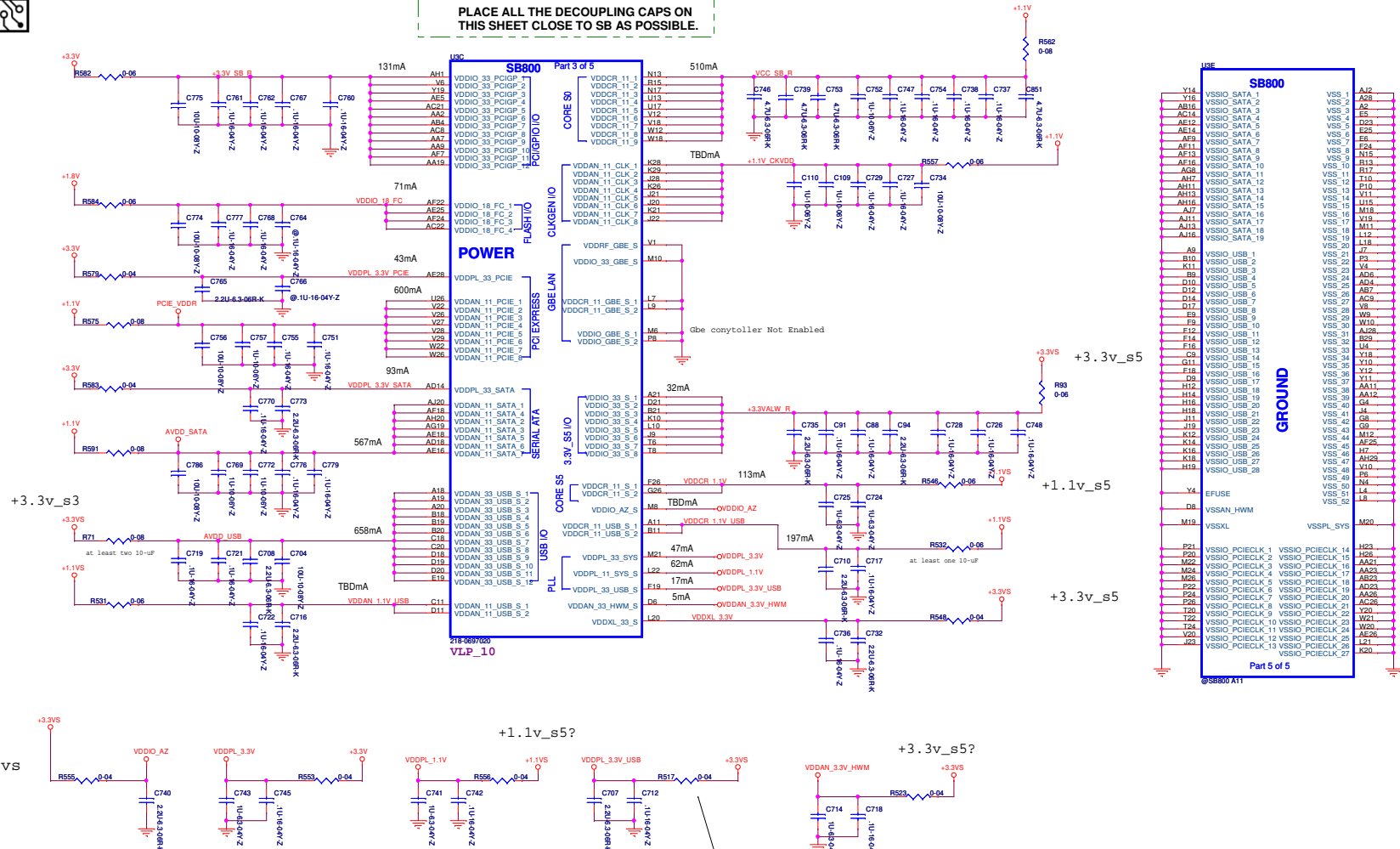
218-0697020

VLP_9





PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



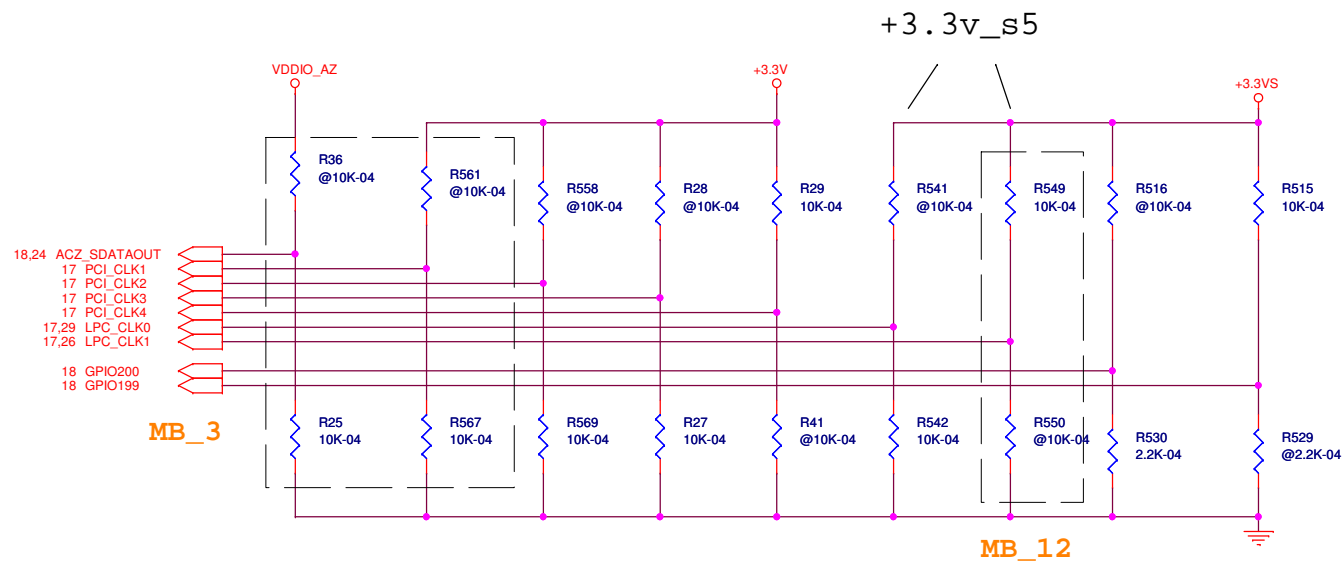
del 1.5vs

+1.1v_s5?

+3.3v_s5?

To meet SB800 SCL1.02:
Separate ferrite bead is not
required for VDDPL_33_USB_S,
Del B603/600ohm bead.

HWM if as GPIO ,caps not use

**REQUIRED STRAPS**

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

low power mode
is not supported
on SB8XX

for int clk
only

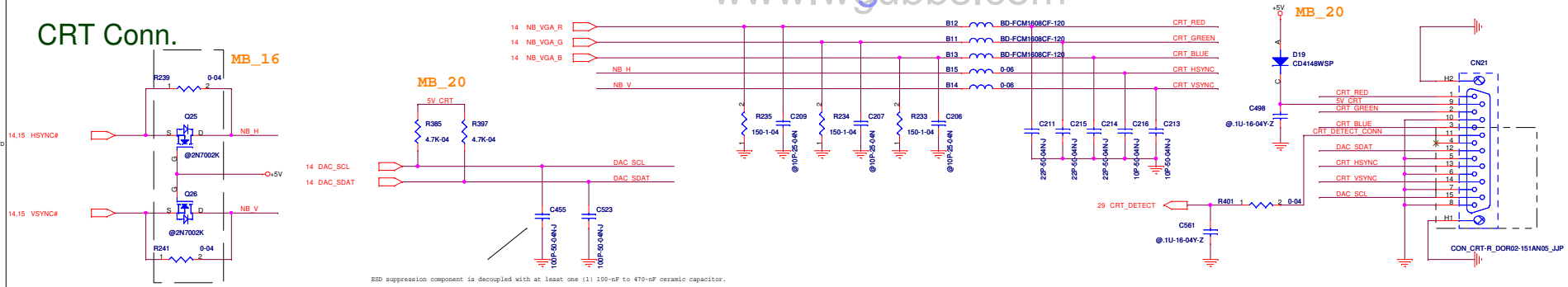
check list write
LL FWH
LX LPC
XL SPI
XX RSVD
(do'nt need pull HI)

FWH are connect vis SIO

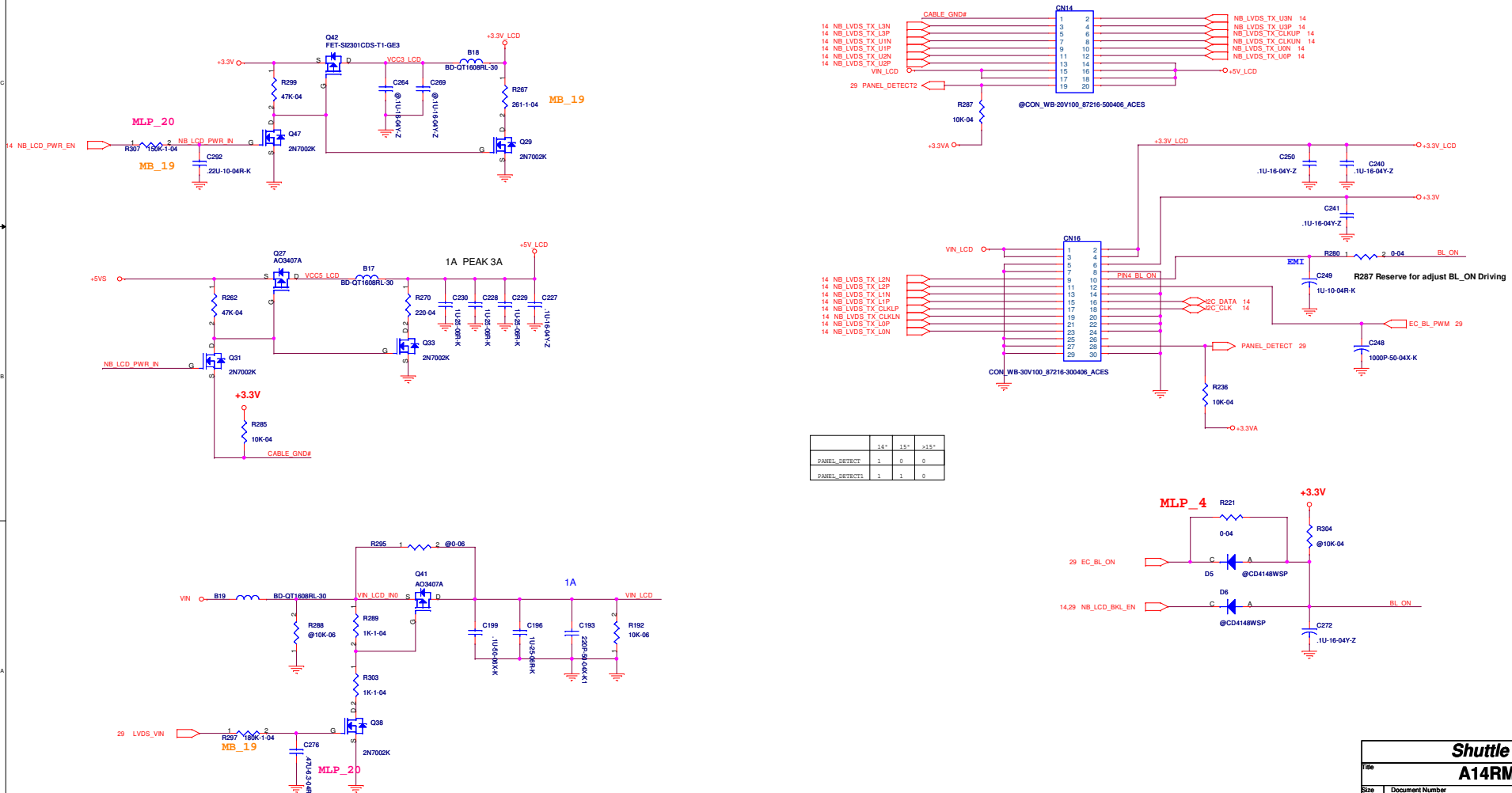
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CRT Conn.

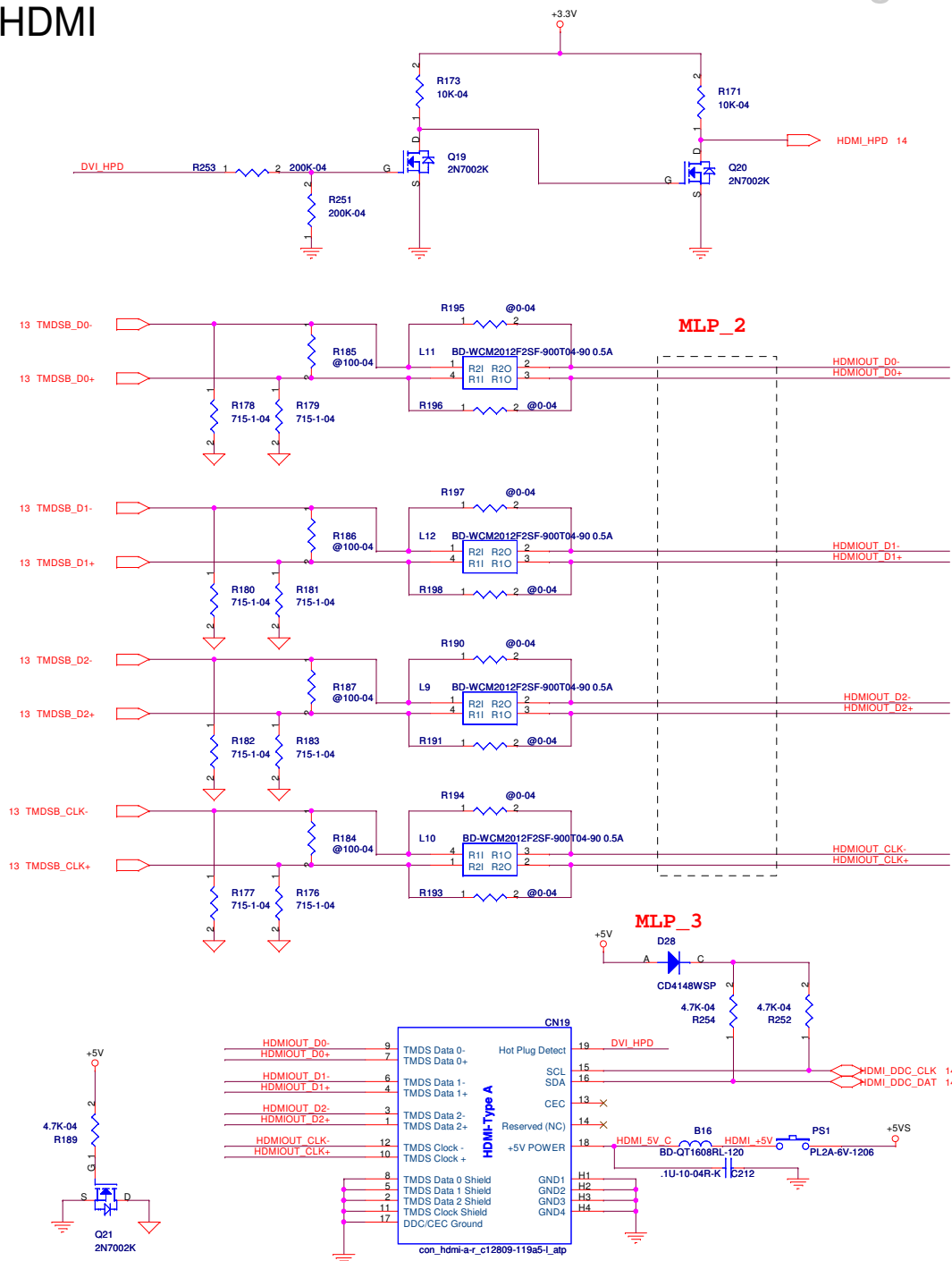


LVDS Conn.

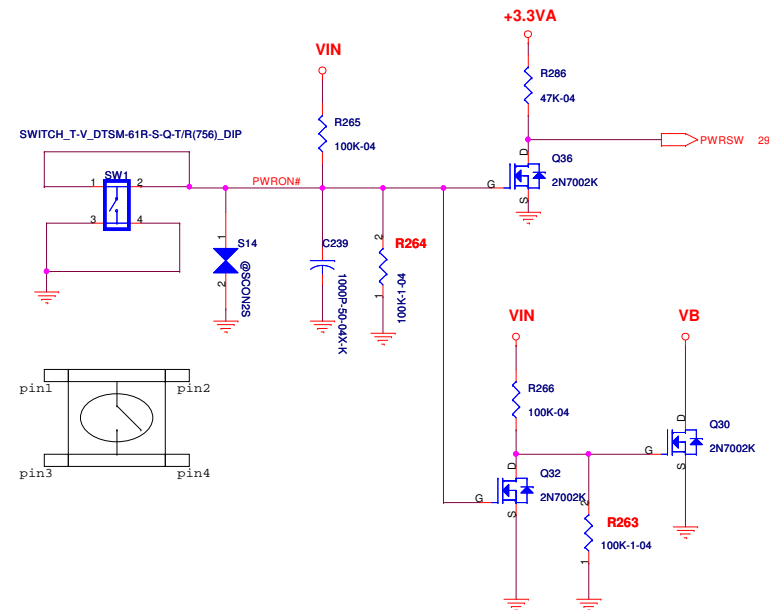


	14"	15"	>15"
PANEL_DETECT	1	0	0
PANEL_DETECT1	1	1	0

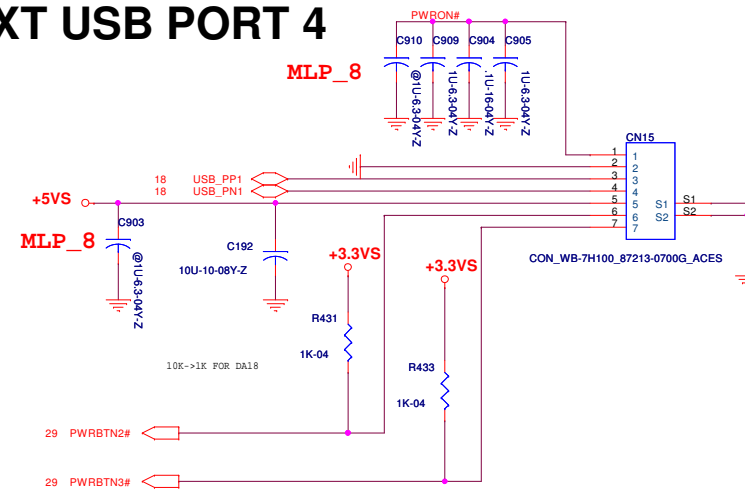
HDMI



PWR SW

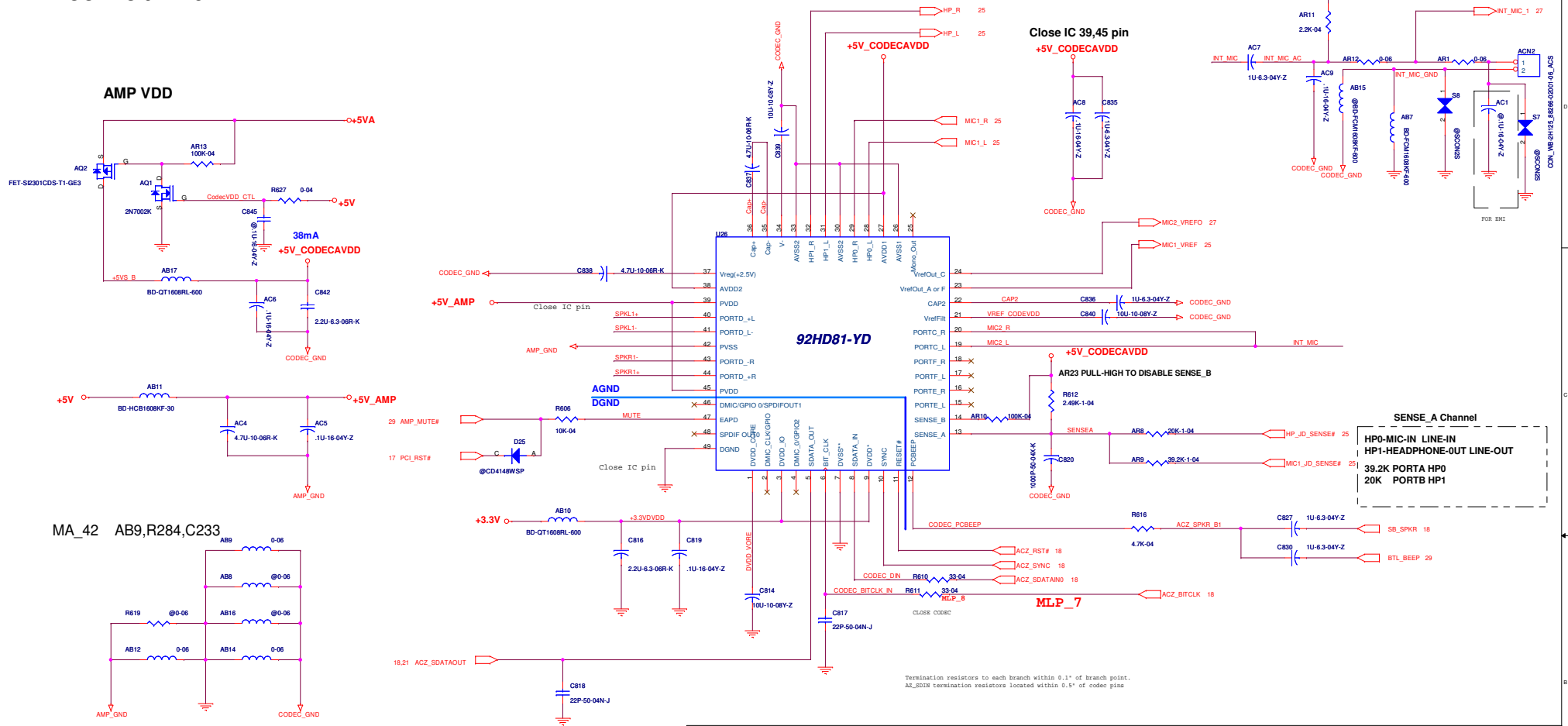


EXT USB PORT 4

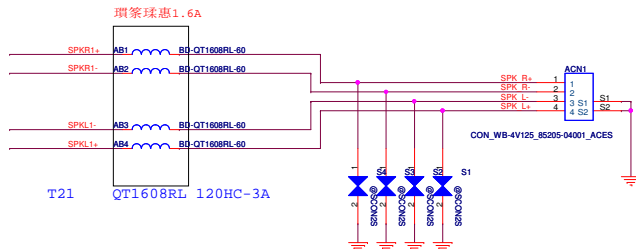


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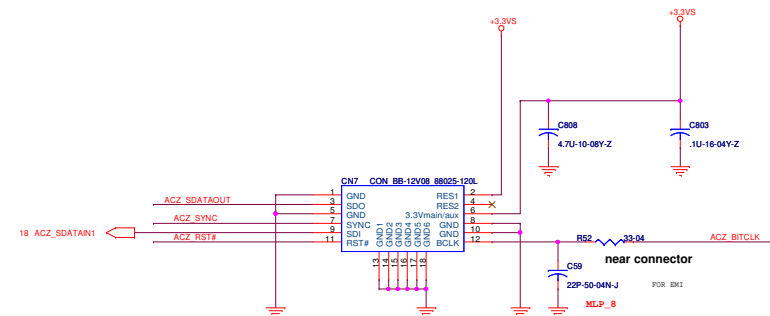
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Custom	HDMI (CH7318C)		1.0
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CODEC 92HD81

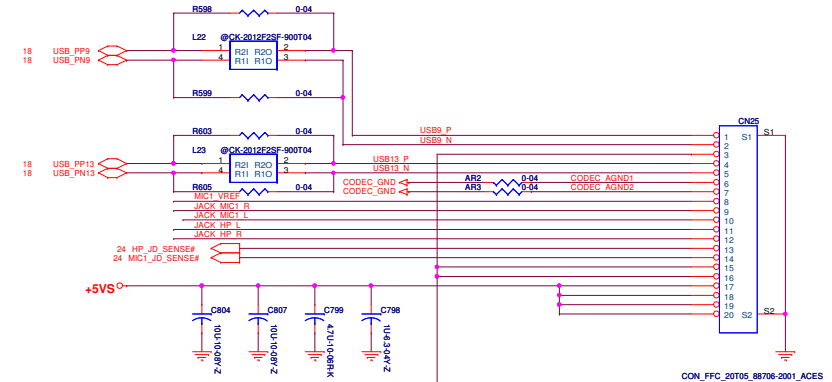
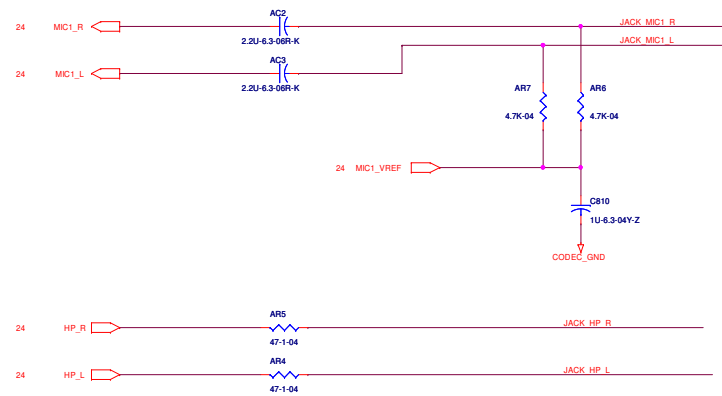
INT_SPEAKER



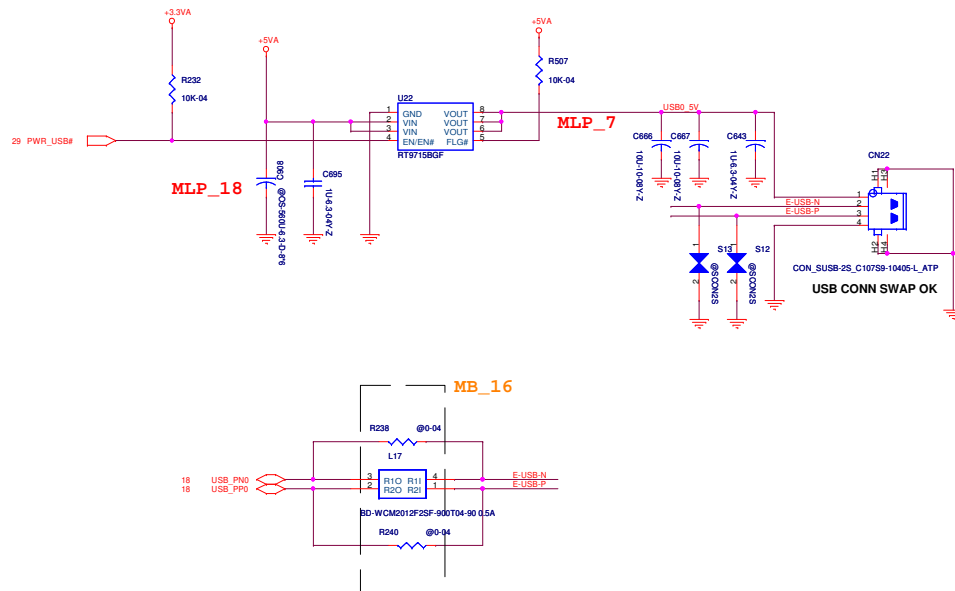
MDC



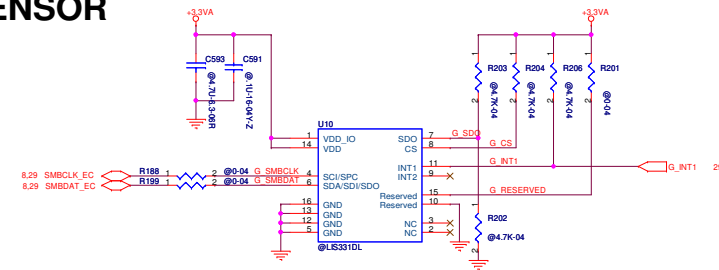
EXT MIC/EXT Line In/ EXT USB JACK



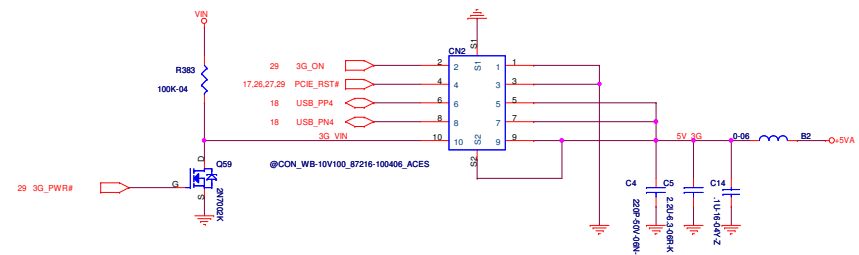
ENHANCE USB Port



G-SENSOR



3G_D/B

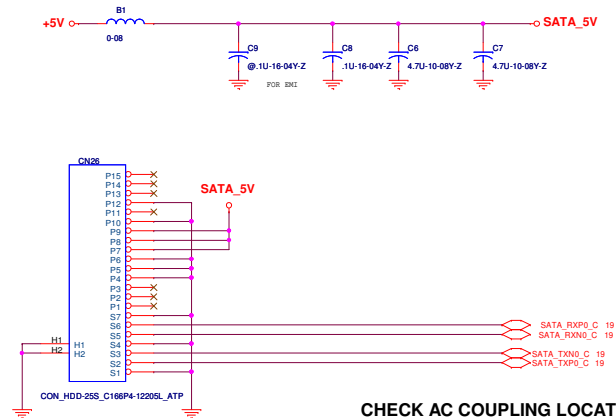


CON_WB-10V100_87216-100406_ACES is
SAME type as LVDS

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Size	Document Number	Rev	
Custom	EXT_MIC/H_P/USB/FAN/G-SENSOR/3G	1.0	
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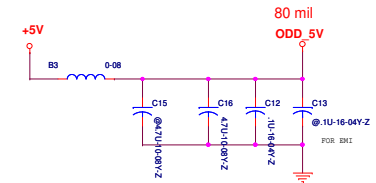
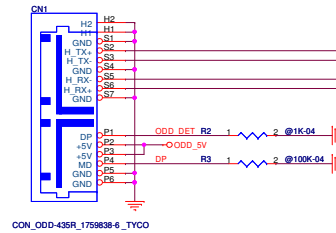
SATA-HDD

1A

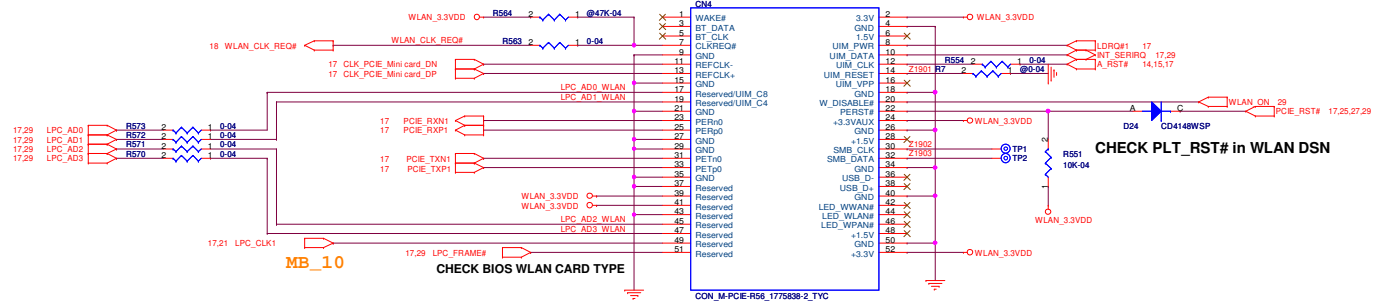
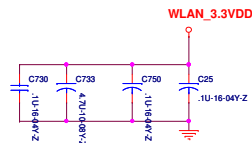
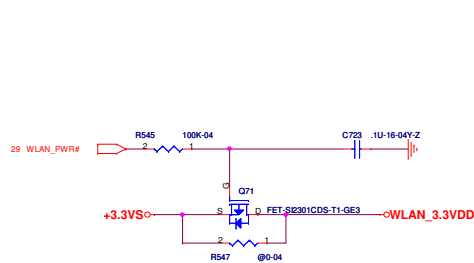


CHECK AC COUPLING LOCATION
REFERENCE DG P316

CD-ROM



MINI CARD CONN

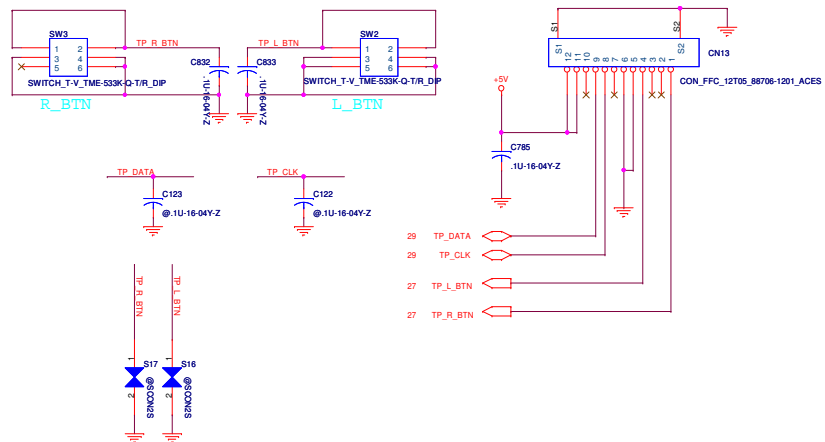


CHECK PLT_RST# in WLAN DSN

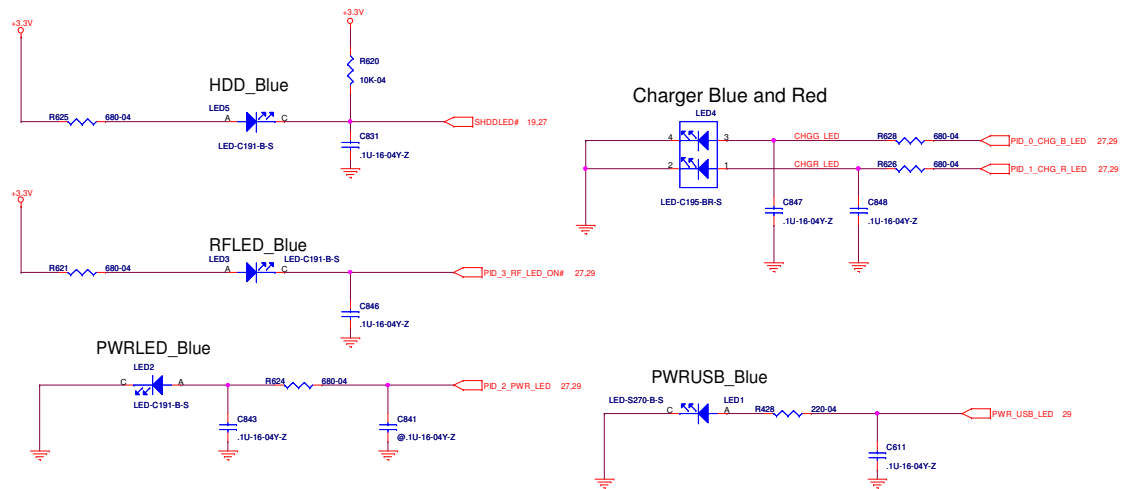
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File	Document Number	Rev
Size	HDD/ODD/MINI CARD	1.0
Date	Monday, October 18, 2010	Sheet 26 of 27

Touch Pad

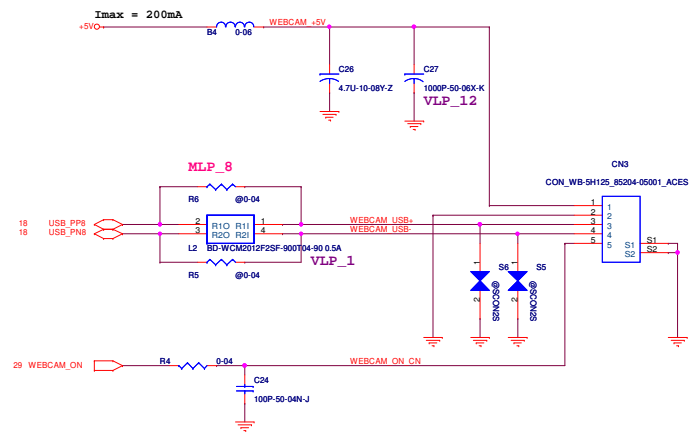


LED

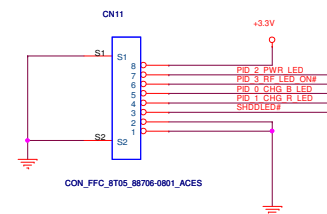


WEBCAM CON

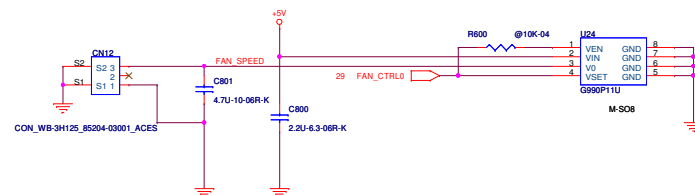
WEBCAM_ON	
1	ON
0	OFF



LED BD



FAN CONTROLLER





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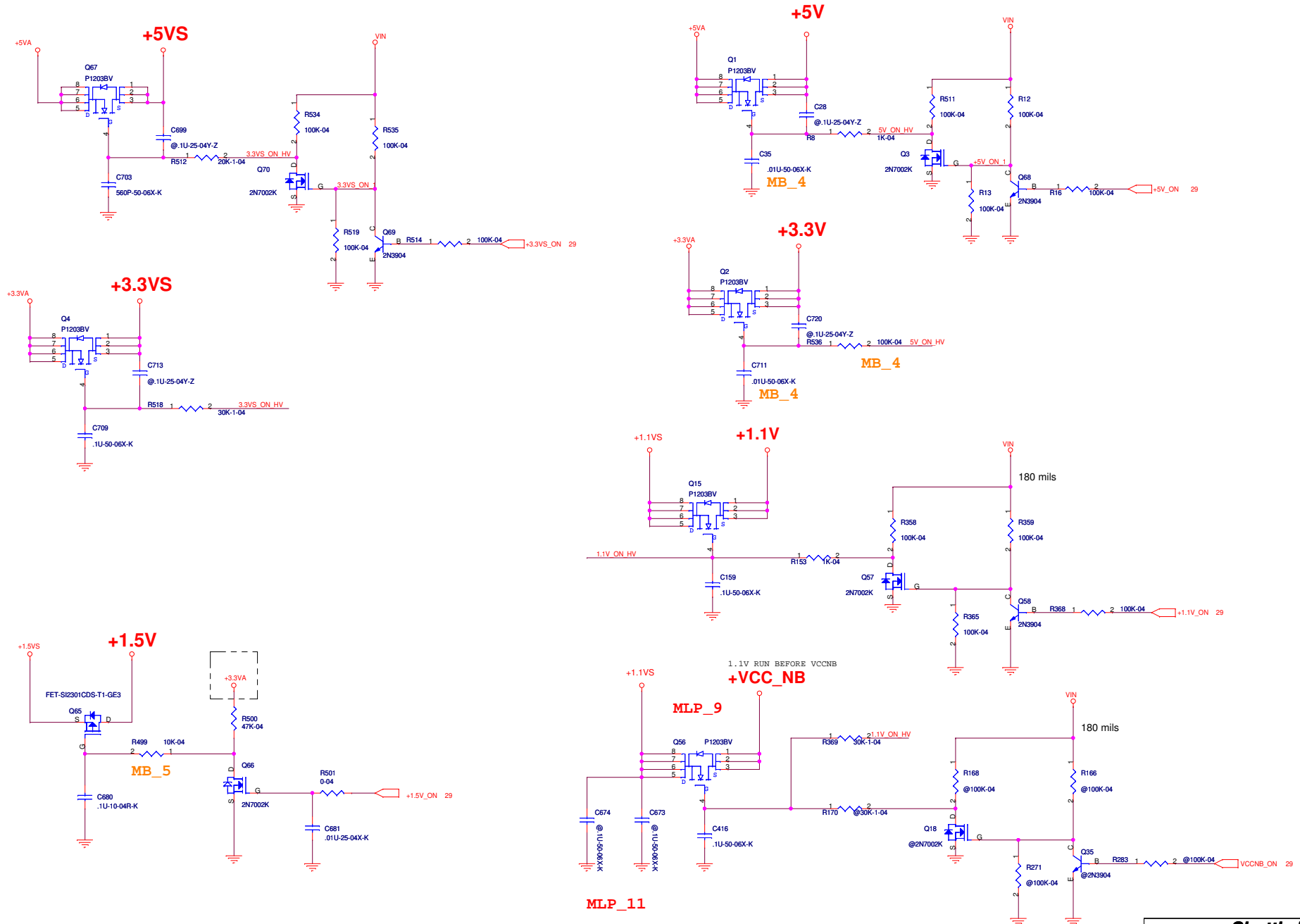


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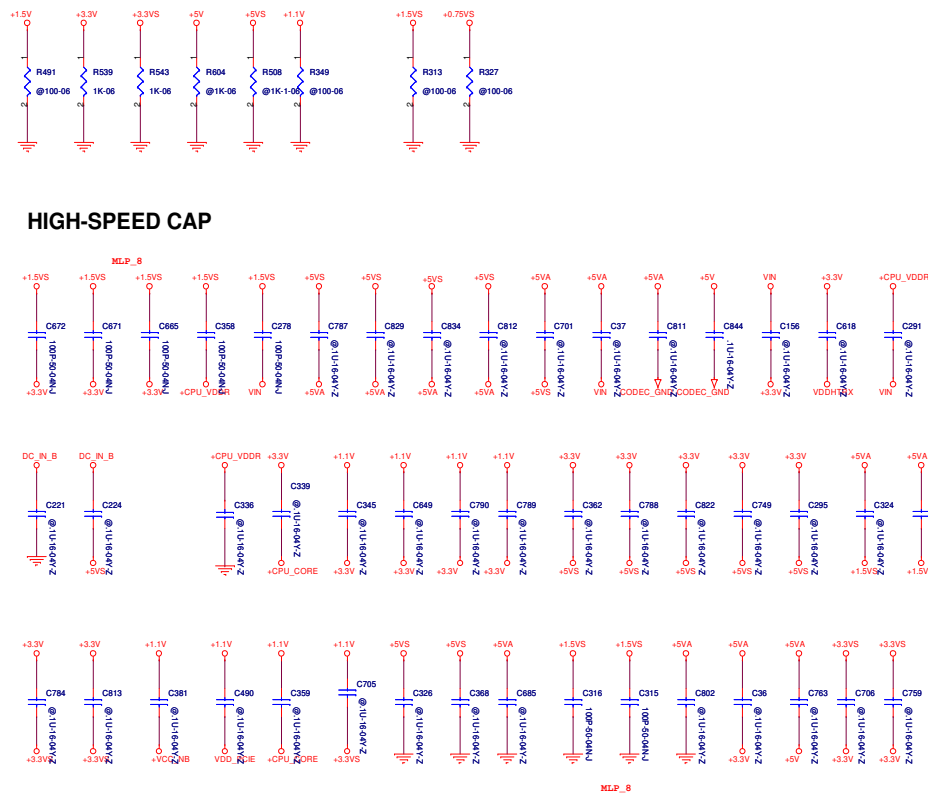
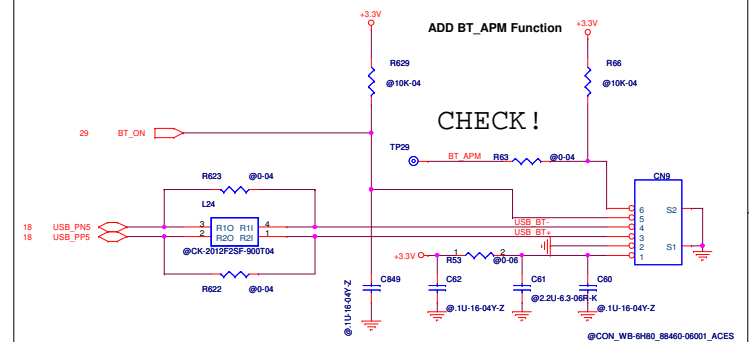
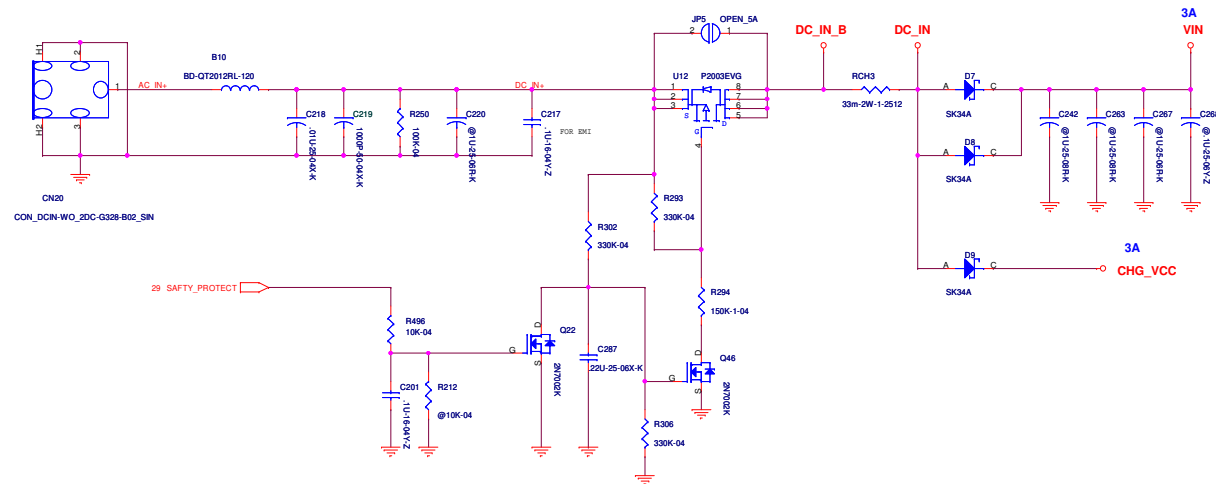


1

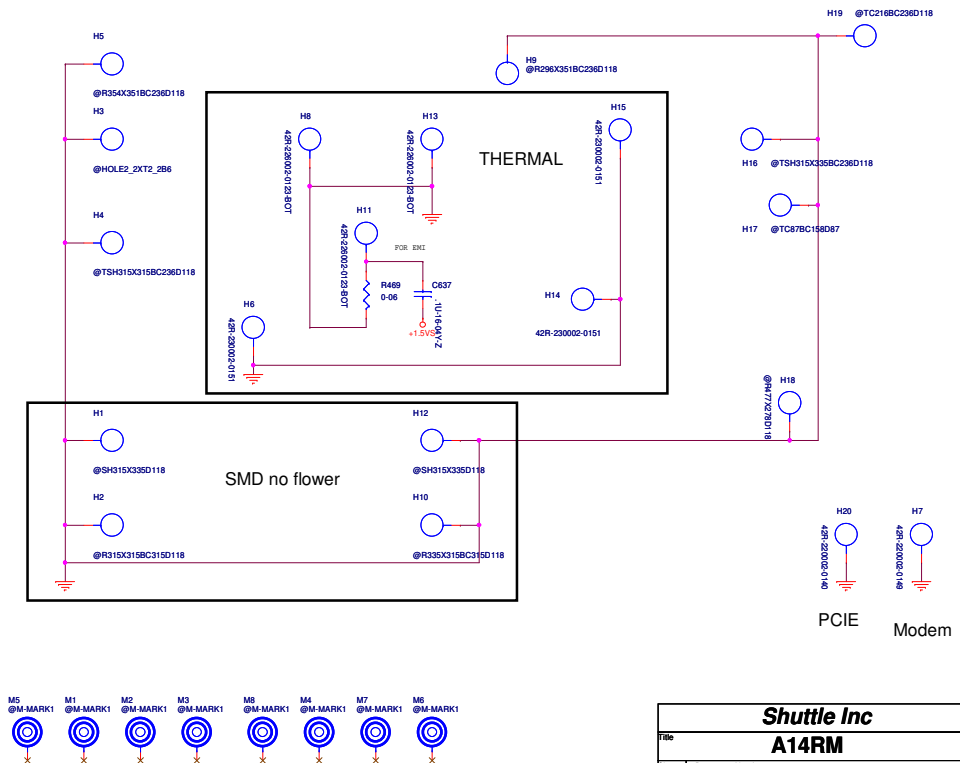
VCCSW



BT CONN

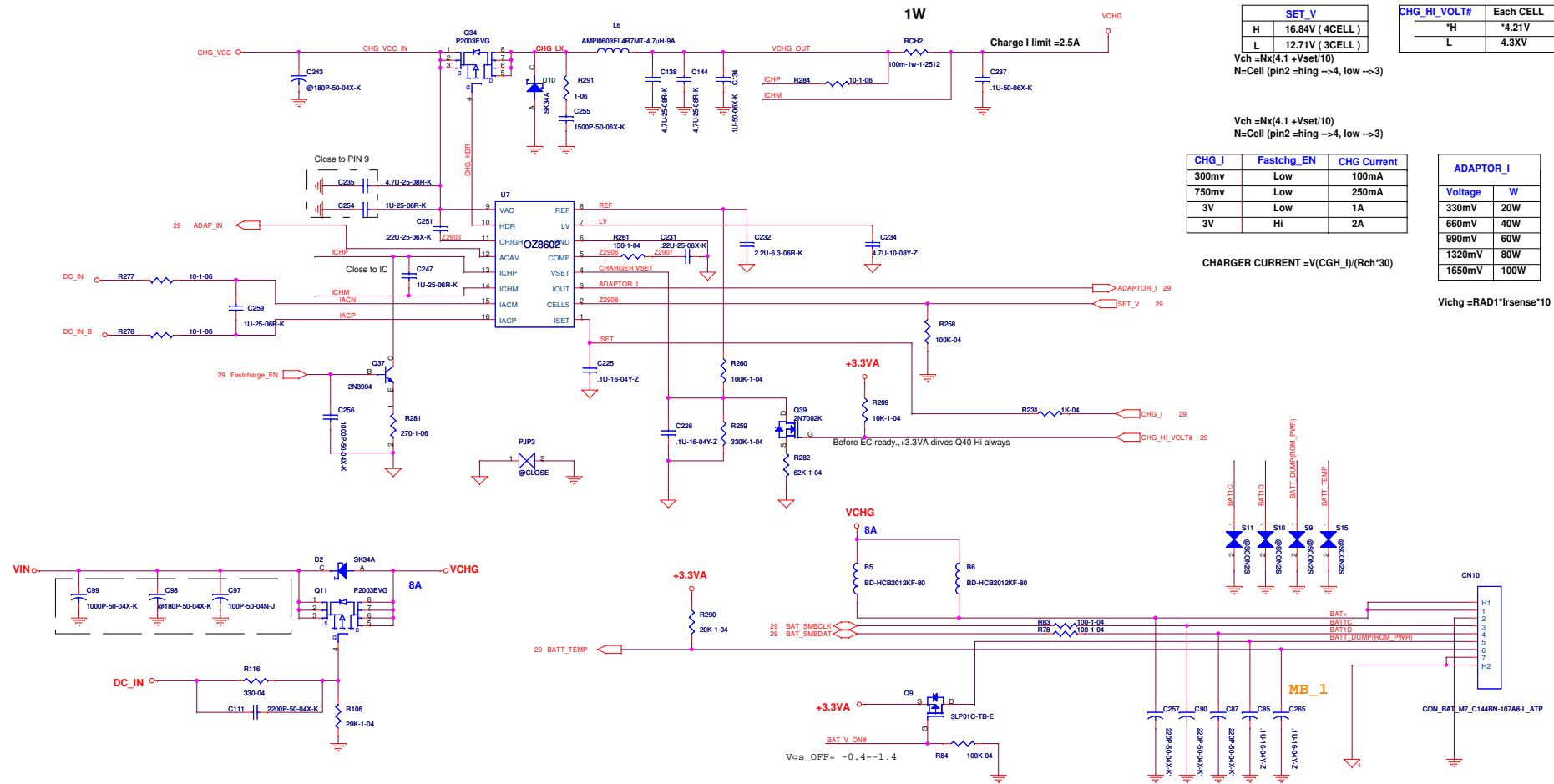


Screw holes

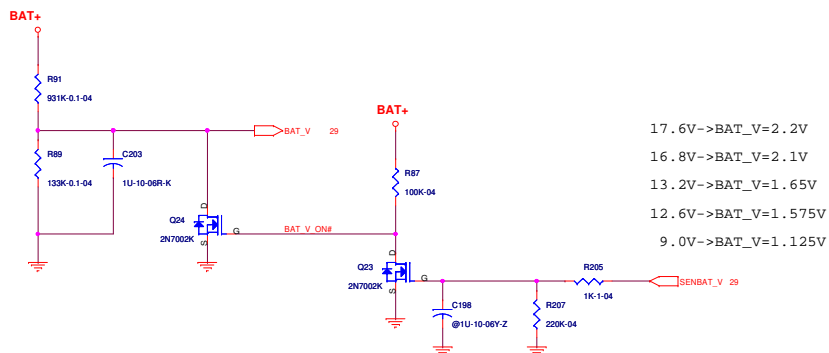


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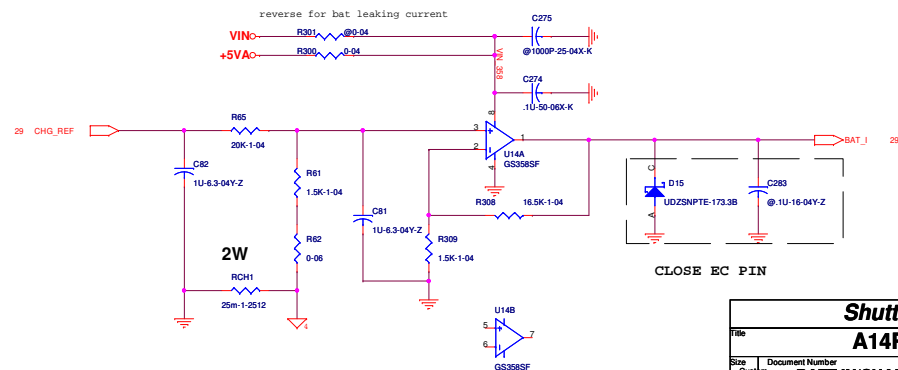
Size Custom	Document Number DC IN/MDC/BT/D-Resistor	Rev 1.0
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Battery Voltage Detect

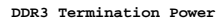
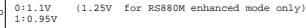


Charge / Discharge Detect



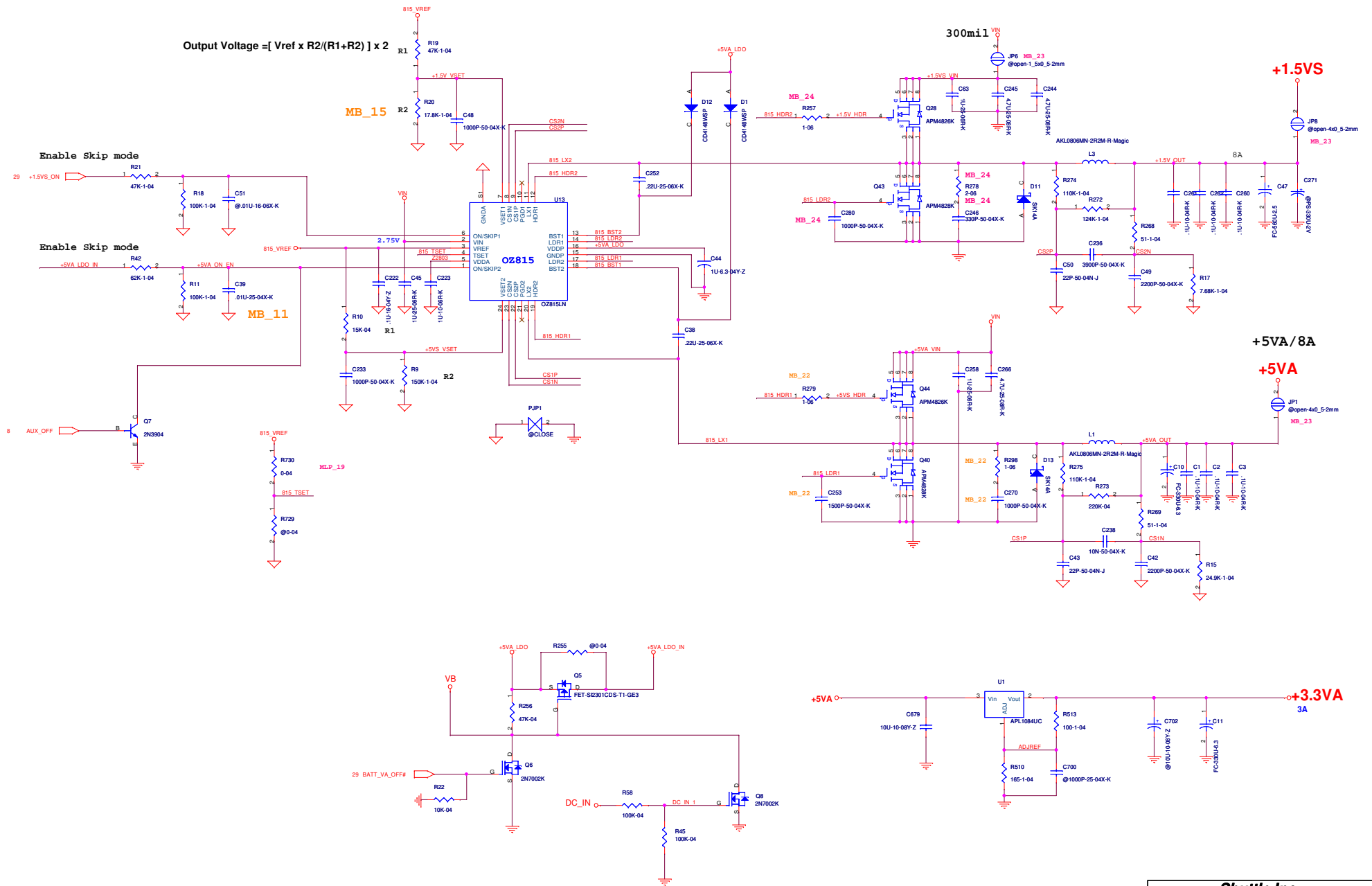


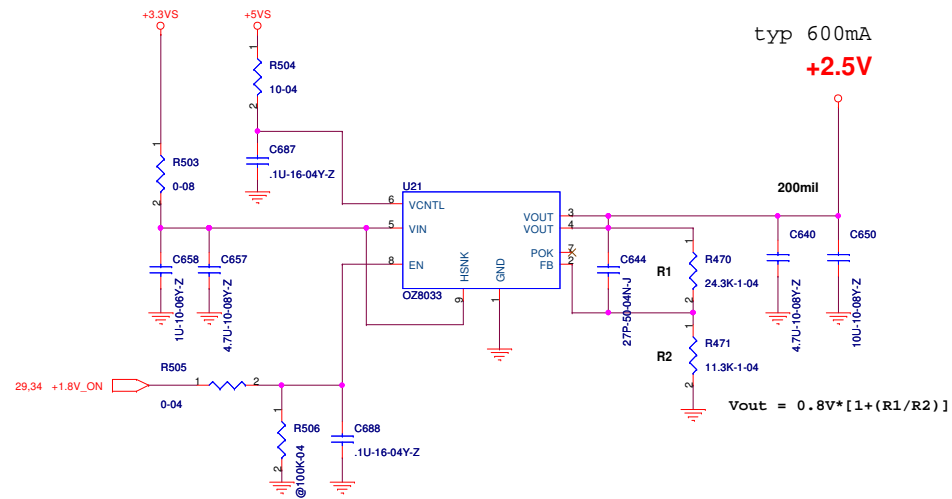
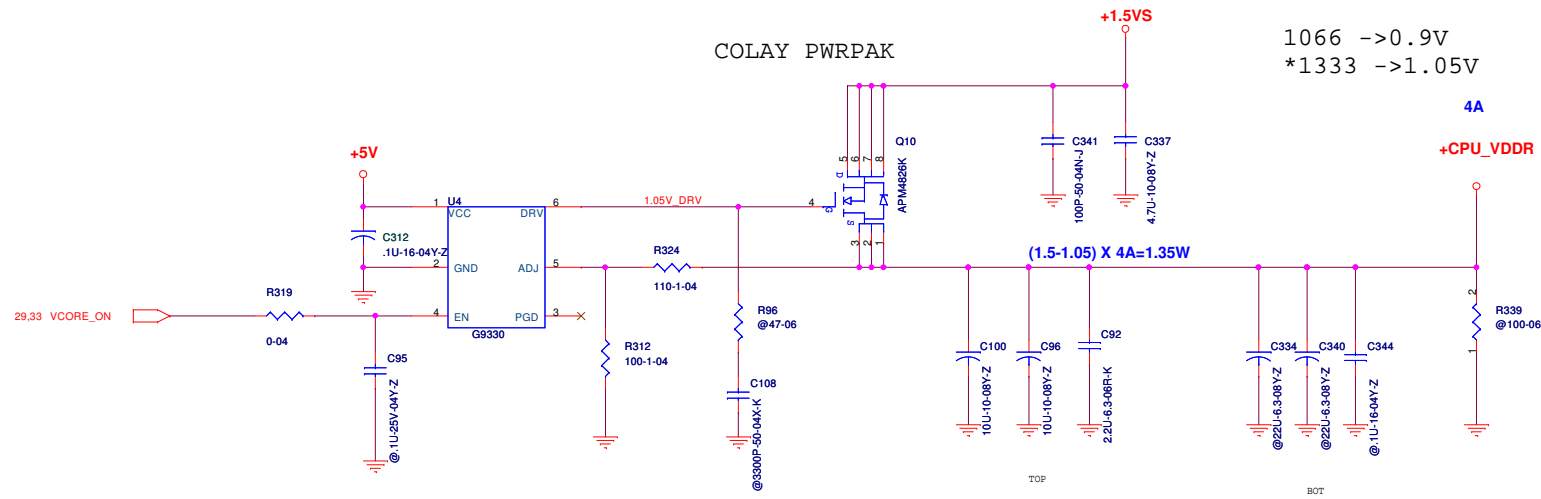
Shuttle Inc			
A14RM			
Document Number	CPU CORE		Rev 1.0
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$$\text{Output Voltage} = [V_{\text{ref}} \times R2 / (R1 + R2)] \times 2$$





RA1 change list:**ECR_A1**

MB_1 P17, P29, P32,modify FOR EMI

MB_2 P33. Vcore pwm Agnd connect Dgnd

MB_3 P21. R36 op, R25 10k set performance mode
R561 op,R563 10k set PCIE gen1

MB_4 P30,C35,C711 change to 0.01u for power sequence

MB_5 P30,R499 10K for 1.5V rise time too short

MB_6 P14,R409 OR PCIE PLL PWR

MB_7 P15,debug bus set ,pull hi level modify

MB_8 P5, open clk R102 R105 R86. X

MB_9 P18, R32 change 0R

MB_10 P26,debug clk P29,EC CLK Change form SB
P17, ADD R700 R701 FOR LPC CLK

MB_11 P35,C38 0.1uF for plug AC ,VIN stack up

MB_12 P17,P14,P27,P21,P18 modify INT CLK GEN

MB_13 P33,P5,P18,DEL EXT CLKGEN

MB_14 change Value R593(0R)

MB_15 P11,P34,P35,SMT bug

MB_16 P22,P25, modify for signal quality

MB_17 P18,P29 reverse EC_EXTSCI#

MB_18 P8, for 3.3V leakage currnt

MB_19 P22, modify for LVDS sequence

MB_20 P22, for 5V leakage currnt

MB_21 P18,pull Hi change to +3.3VS

MB_22 P33, power solution

VLP_1,P28 value of common choke

VLP_2,P12 value of RS880

VLP_3,P13 value of RS880

VLP_4,P14 value of RS880

VLP_5,P15 value of RS880

VLP_6,P16 value of RS880

VLP_7,P16 value of RS880

VLP_8,P17 value of SB800

VLP_9,P19 value of SB800

VLP_10,P20 value of SB800

VLP_11,P18 value of SB800

ECR_A1,P18 Add R715 0ohm for lan D3 sent by EC

2010/10/18

VLP_12,P28 C27 change value

RB change list:

MB_23 JUMP modify

MB_24 power solution p33,p34,p35

MB_25 P8,prochot modify add Q72

MB_26 P27,P17 crystal change smt type

MB_28 P29,add NB_LCD_FWR_EN to EC

RLP change list: **MLP_1**

MLP1 P27,R716 modify value 0-04 for lan 25Mhz

MLP2 P23,delete HDMI reserve resistance

MLP3 P29,P8,P23 SMBUS leaking current.

MLP4 P22,R221 don't colay change to 0402

MLP5 P29,ADD C852 for BATT_TEMP for stable signal

MLP6 P11,modify value change CAP for DDR stability

MLP7 P18,del 0 ohm

MLP8 P18,24,10,23,28,31 ,EMI SOLUTION

MLP9 P30,del JP4

MLP10 P31,del R350

MLP11 P30,add two cap for 1.1V PWM

MLP11 P34,Modify choke & value for 1.1v pwm

MLP12 P29,reserve 0ohm for 8380A

MLP13 P23, CMOS clear Jump move

MLP14 P27, LAN modify

MLP15 P29, 1.2vs_on reserve

MLP16 P27, LAN d3 mode

MLP17 P33, add C906 C907 for OS idle nosie

MLP18 P25, reverse c908 for USB plug power off issue

MLP19 P34,P35 ADD R727 R728 for 1.1V freq, ADD R728 R729 For 5V freq.

MLP20 P22, Modify for lvds sequence

MLP21 P27, LAN CLK MODIFY

MLP22,P25 3G conn del